ABSTRACT

Title of dissertation: NANOCRYSTALLINE DIAMOND THIN FILM INTEGRATION IN AlGaN/GaN HIGH ELECTRON MOBILITY TRANSISTORS AND 4H-SiC HETEROJUNCTION DIODES

Marko Jak Tadjer, Doctor of Philosophy, 2010

Dissertation directed by: Professor John Melngailis
Department of Electrical Engineering

The extremely high thermal conductivity and mechanical hardness of diamond would make it the natural choice for device substrates when large area wafer production becomes possible. Until this milestone is achieved, people could utilize nanocrystalline diamond (NCD) thin films grown by chemical vapor deposition (CVD). A topside thermal contact could be pivotal for providing stable device characteristics in the high power, high temperature, and high switching frequency device operating regime that next-generation power converter circuits will mandate. This work explores thermal and electrical benefits offered by NCD films to wide bandgap semiconductor devices. Reduction of self-heating effects by integrating NCD thin films near the device channel of AlGaN/GaN high electron mobility transistors (HEMTs) is presented. The NCD layers provide a high thermal conductivity path for the reduction of hot electron dispersion, a phenomenon caused by self-heating and detrimental to the continuous operation of GaN devices in power switching circuits.

Recent advances in diamond doping have made it possible to think of this material as a very wide bandgap semiconductor (5.5 eV for ideal diamond). A few unique properties, such as negative electron affinity (χ = -0.2 eV for H-terminated diamond), make this material very interesting. Using H-terminated NCD, a heterojunction with 4H-SiC has been developed. Undoped and B-doped NCD were deposited on both n^- and p^- 4H-SiC epilayers. Different metals were studied to provide an Ohmic contact to the NCD layer. I-V measurements on p^+ NCD / n^- 4H-SiC p-n junctions indicated Schottky rectifying behavior with a turn-on voltage of around 0.2 V. The current increased over 8 orders of magnitude with an ideality factor of 1.17 at 30 ℃. Ideal energy-band diagrams suggested a possible conduction mechanism for electron transport from the SiC conduction band to either the valence band or Boron acceptor level of the NCD film. Cathodoluminescence and thermally stimulated current methods were employed to study the deep level assisted conduction in this heterojunction. Applications as a simultaneous UV-transparent optical and Schottky electrical contact to 4H-SiC are discussed.

NANOCRYSTALLINE DIAMOND THIN FILM INTEGRATION IN AlGaN/GaN HIGH ELECTRON MOBILITY TRANSISTORS AND 4H-SiC HETEROJUNCTION DIODES

by

Marko Jak Tadjer

Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
2010

Advisory Committee:
Professor John Melngailis, Chair
Professor Martin Peckerar
Professor Timothy Horiuchi
Professor Agis Iliadis
Professor Lourdes Salamanca-Riba, Dean's Representative
Dr. Karl Hobart, Special Member, Naval Research Laboratory

Preface

This dissertation is organized in seven chapters, based on the publications listed below. Chapter 1 provides background information and the key contributions of this research. Chapter 2 reviews the relevant III-Nitride literature, provides some theoretical background on AlGaN/GaN HEMTs, practical considerations for device fabrication, as well as some past research in GaN device fabrication. Chapter 3 is based on NCD integration in HEMT devices, and chapter 4 provides further insight into HEMT surface passivation. Chapter 5 focuses on nanocrystalline diamond (NCD) growth, processing, and electrical characterization. Section 6.1 studies the properties of NCD/4H-SiC heterojunctions, and section 6.2 focuses on bulk trap properties of 4H-SiC. Chapter 7 concludes this dissertation and gives suggestions for future research.

Chapter 2:

- T. J. Anderson, M. J. Tadjer, M. A. Mastro, J. K. Hite, K. D. Hobart, C. R. Eddy Jr., and F. J. Kub, "An AlN/ultrathin AlGaN/GaN HEMT Structure for Enhancement Mode Operation," IEEE Electron Dev. Lett., vol. 30, no. 12, pp. 1251, 2009. Presented at the Electronic Materials Conference (EMC), Penn State University, 2009.

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Chapter 4:

- M. J. Tadjer, T. J. Anderson, K. D. Hobart, M. A. Mastro, J. K. Hite, J. D. Caldwell, Y. N. Picard, F. J. Kub, and C. R. Eddy, Jr., "Surface Passivation Comparison using in-situ and ex-situ deposited SiN_x on AlGaN/GaN High Electron Mobility Transistors," Journal of Electronic Materials, 2009, under review. Presented at EMC 2009.

Chapter 5:

- M. J. Tadjer, T. J. Anderson, K. D. Hobart, T. I. Feygelson, J. E. Butler, and F. J. Kub, "Comparative Study of Ohmic Contact Metallizations to Nanocrystalline Diamond Films," Mater. Sci. Forum, vols. 645-648, pp. 733, 2010. Presented at ICSCRM 2009.

Chapter 6:

- M. J. Tadjer, K. D. Hobart, J. D. Caldwell, J. E. Butler, K. X. Liu, C. R. Eddy Jr., D. K. Gaskill, K. K. Lew, B. L. VanMil, R. L. Myers-Ward, M. G. Ancona, F. J. Kub, and T. I. Feygelson, "Nanocrystalline Diamond Films as UV-Semitransparent Schottky Contacts to 4H-SiC," Appl. Phys. Lett. 91, 163508 (2007). Presented at EMC 2007, South Bend, IN.

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To my growing family.

Acknowledgments

I am grateful to my advisor at the University of Maryland, Professor John Melngailis, for letting me pursue my academic freedom while challenging my thinking process with his questions. Thank you for making extra effort to be there for me every time I looked for you, even back in 2003 when you still didn't know me.

Many people have taken a chance by working with me over the years, but only at Dr. Karl Hobart's group at NRL have I been able to find the perfect research environment to let me learn the profession and grow to understand it better. For his mentorship over the past four years, I am eternally grateful to him and the rest of the team: Dr. Fritz Kub for whom inventing is like breathing, Dr. Travis Anderson for teaching me the tricks of HEMT fabrication, Dr. Joshua Caldwell for his superior understanding of physics, Dr. Robert Stahlbush for teaching me how to approach a problem meticulously from start to finish, and Dr. Eugene Imhoff for knowing a lot about everything. I must mention Dr. Michael Mastro, Dr. Chip Eddy, and the rest of the MOCVD growth gurus, as well as Dr. Tanya Feygelson and Dr. Jim Butler, without whom literally none of the samples would have materialized. Thanks to Dr. Loretta Shirey, Mr. Milt Rebbert, and the NRL Nanoscience Institute staff for equipment and process support. Corporate support in the form of wafers (Nitronex, Inc.), device samples (Cree, Inc.) and processing support (GE Global Research) needs to be recognized as well. Cathodoluminescence measurements were performed by Dr. Leonard Brillson and Greg Sollenberger at the Ohio State University. The complete list of people (at NRL or elsewhere) from

whom I have learned over the years is too long to enumerate; it must suffice to be grateful to the U. S. Government (and Thomas Edison) for creating a place where knowledge can be found a few doors down the hallway. Thank you for being where you were, doing what you did.

Special gratitude to the members of the dissertation committee: Dr. Martin Peckerar, Dr. Timothy Horiuchi, Dr. Agis Iliadis, and Dr. Salamanca-Riba. The administrative support of Dr. Tracy Chung and Mrs. Maria Hoo at the ECE Department was essential as well.

Kudos to The Kids: Elena, Ina, Nick the Greek, Stephan, and Vesi, for being the perfect bunch to relax with after a long day in the lab.

My family has always believed in me and supported anything I've done. I will never quit trying to draw us closer from across oceans, countries, cultures, and languages. I love you mom, and I promise to call you more often.

My deepest gratitude goes to Dr. Grecia Lapizco Encinas, whom I have the privilege to call my wife. Thank you for your love and support during these stressful times, and for LaTeX. Your presence in my life has made this dissertation infinitely more satisfying.

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List of Abbreviations

NCD	nanocrystalline diamond
MOCVD	metal organic chemical vapor deposition
PECVD	plasma enhanced chemical vapor deposition
MBE	molecular beam epitaxy
HPHT	high pressure high temperature
HEMT	high electron mobility transistor
2DEG	two dimensional electron gas
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
AccuFET	accumulation mode field effect transistor
MOSCAP	metal oxide semiconductor capacitor
ALD	atomic layer deposition
SEM	scanning electron microscopy
AFM	atomic force microscopy
CL	cathodoluminescence
PL	photoluminescence
EL	electroluminescence
RIE	reactive ion etching
ICP	inductively coupled plasma
IPA	isopropanol
SC-1	standard cleaning solution no. 1
SC-2	standard cleaning solution no. 2
DI	deionized water
TLM	transfer length method
CV	capacitance-voltage
IV	current-voltage
TSC	thermally stimulated current
EMC	Electronic Materials Conference
ICSCRM	International Conference on Silicon Carbide and Related Materials
ISDRS	International Semiconductor Device Research Symposium
NRL	Naval Research Laboratory

Chapter 1

Introduction

1.1 Background and Motivation

Modern applications require ever more powerful and more efficient power delivery systems. Hybrid vehicles require more efficient converters to better utilize battery usage. Modern computer processors can generate current transients in excess of 100 A/μs. Soldiers in the field, whose safety we recognize as a top priority, can choose among a plethora of wearable gadgets, which they wear along with the power supply. The omnipresent demand in the field of electrical engineering for cheaper, lighter, faster, more powerful, and more efficient electronic systems is the main driving force behind the research in power electronic devices. Silicon has been the material of choice in over 99 % of transistors manufactured, and the transistor is the one artifact mankind has produced in largest quantities throughout its existence. However, there is a small niche of applications for which the properties of Si fall short.

Due to their wide energy gap, thermal conductivity, and blocking voltage, materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have been explored in recent years in power switching applications. GaN power transistors have been demonstrated to block 1.5 kV, and SiC power transistors can withstand more than 10 kV in forward blocking mode [11]. However, ability to withstand high elec-

tric fields is not the only determining factor in choice of devices. Effective field termination strategies have enabled Si-based power IGBTs to be rated up to 6.5 kV. However, operation in power switching converters requires fast switching with minimal losses. The high critical field of 4H-SiC enables relatively thin epitaxial vertical devices to be fabricated with low resistance in the drift region, which greatly reduces the switching power losses of the device. On the other hand, lateral III-Nitride HEMTs possess ultralow channel resistance due to the presence of a two-dimensional electron gas (2DEG). Combined with the low parasitic capacitances enabled by a semi-insulating substrate, III-Nitride based power HEMTs have been demonstrated to switch in the MHz regime in boost converter applications.

One of the great advantages of SiC has been the existence of SiO_2 as a native oxide. However, the quality of thermal SiO_2 grown on SiC has not been as good as that grown on Si. In fact, recent research has shown that deposition of SiO_2 on GaN using low pressure chemical vapor deposition (LPCVD) produces a more stable interface than on SiC by reducing the interface state density to $3.8\text{x}10^{10}$ cm^{-2} at energy offset of 0.19 eV away from the conduction band edge [17]. Therefore, GaN should not be counted out of the race just because it does not possess a native oxide.

In addition to the choice of material, currently wide-bandgap researchers have to choose the type of device they propose for a power switch. The dominant structure in industry, the MOSFET, due to the requirements of a stable oxide and high breakdown voltage, has been seriously challenged by the bipolar junction transistor (BJT), the junction field effect transistor (JFET), the insulated-gate bipolar tran-

sistor (IGBT), and the HEMT. BJT devices do not need an MOS interface and therefore bypass the oxidation problem altogether. However, base resistance reduction, which is directly related to the carrier lifetime, which in turn depends on the material quality, has presented its own set of challenges for these devices. On the other hand, GaN-based majority-carrier HEMT structures have been demonstrated to enable higher breakdown voltages, faster reverse recovery, a smaller form factor, and lower R_{ON}-Q_G (on resistance - gate charge) product than the present state-of-the-art Si technology. This ultimately results in smaller, higher efficiency power converters where the lower losses directly translate to lower heating and therefore less need for bulky cooling schemes.

A major advantage for GaN and SiC is the extremely fast RF switching devices these materials enable. GaN-based HEMT devices with low on resistance, high on-state current, and low noise profile have found application in wireless transmitter hardware. In the power switching segment class AB or B operation necessitates high quiescent drain voltage operation in order to achieve high efficiency. Output impedance matching is ensured by the high output power achieved by increasing the output voltage, not the output current. This step also avoids placing several devices in parallel, which is a common tactic in Si-based electronics. [18]

Current research in GaN-based power switching converters report device switching frequencies of around 1 MHz. For comparison, Si power MOSFETs usually switch in the kHz regime. DC-DC converter circuit designers employ techniques such as multiphase topography and sophisticated pulse-width modulation to increase the efficiency of the converter. On the other hand, 2-7 % increases in efficiency have

been measured solely by substituting a Si power device with a GaN or SiC ones. The cost reductions due to the simplified circuit design process could offset the higher device cost, resulting in faster technology adoption.

The question of whether Si, GaN, or SiC will dominate the power electronics market is probably best answered by the market itself. Commercial GaN HEMTs and up to 1.2 kV SiC Schottky diodes devices are already available for sale by both Cree and Infineon. The latter's parent company, Siemens, has commercialized a motor drive inverter using SiC diodes. In addition, hybrid technologies marrying Si and SiC technology are being brought to market as well. As larger area substrates become available, we can expect to see wide bandgap devices establish themselves in power switching applications.

1.2 Key Contributions

- Integration of nanocrystalline diamond (NCD) heat spreading layers in AlGaN/GaN HEMT devices. Development of a diamond-before-gate process sequence ensured diamond growth (750 ℃, 5 hours) occurred prior to Schottky gate deposition, thus avoiding Schottky gate degradation caused by thermal stress.
  - Demonstration of stable HEMT parameters (sheet resistance, mobility, and sheet carrier density) upon NCD growth induced thermal stress.
  - Development of reliable NCD dry etching process using O_2 ICP.
- Development of improved AlGaN/GaN HEMT surface passivation by growing SiN_x *in situ* during CVD growth. Comparison with non-passivated and traditional *ex situ* passivation with PECVD-deposited SiN_x demonstrated reduced surface state density and improved breakdown voltage.
- Development of enhancement mode III-nitride HEMT devices. This was achieved by using a AlN/thin AlGaN/GaN HEMT structure and an AlN-selective wet etch. The AlN was etched down to the AlGaN layer underneath the gate to leave a depleted channel under the thin (4 nm) AlGaN region, resulting in a threshold voltage of +0.2 V.
  - Control of AlGaN/GaN HEMT threshold voltage was also performed by AlGaN dry etching in the gate region. The advantage of the wet-etch approach by avoiding RIE etch damage in the gate is discussed.

- Demonstration of a HEMT boost converter circuit designed specifically for probing wafer level HEMT devices. This enabled convenient testing of a large number of HEMT devices in realistic conditions (f = 300-800 kHz), without package-added parasitic components, in order to quantify the converter performance and its relationship with the HEMT limitations.

- Development of heterojunction Schottky diodes using p-type NCD and n-type 4H-SiC. This device takes advantage of the UV-semitransparency of NCD to implement a simultaneous electrical and optical contact to 4H-SiC. Bulk trap level characterization of 4H-SiC was performed using thermally stimulated current measurements to help explain trap-assisted NCD/SiC conduction mechanisms.

- Comparison of different metal structures for Ohmic contacts to doped and undoped NCD thin films.

- Development of oxide and bulk trap density spatial separation methods in n-channel 4H-SiC transistors based on thermally stimulated current analysis. To the author's best knowledge, thermally stimulated current measurements on 4H-SiC transistors and pn junctions have not been previously published in the literature.

Chapter 2

High Electron Mobility Transistors

2.1 Literature Review

The following review summarizes the relevant literature in the fields of GaN material development, high electron mobility transistors, and nanocrystalline diamond (NCD) growth and processing. Examined are device results, as well as publications focusing on specific processing challenges.

For GaN technology, these include Ohmic and Schottky contacts, contact annealing, gate dielectrics, etching, ion implantation, implant annealing and isolation, and the role of impurities. Following a general discussion of the GaAs HEMT technology, relevant papers on AlGaN/GaN HEMT devices will be presented.

Gallium Nitride was first synthesized in 1938 by Juza and Hahn by reacting hot Ga with ammonia, which produced needles and platelets of the material [19]. Seventy years later, GaN is being intensely researched as the material of choice for high-breakdown, high-frequency, high-temperature devices. As a direct-gap semiconductor, GaN crystallizes in either the wurtzite (E_G = 3.39 eV at 300 K) or the zinc blende (E_G = 3.2 eV at 300 K) lattice structures [1]. Zinc blende GaN can be epitaxially grown using either molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD). Its main applications are found in blue and UV light emitting diodes, laser diodes, and UV photodetectors, as well as the tran-

sistor devices developed in this work. For n-type conductivity, GaN can be doped with Si, which is a shallow donor residing 0.02-0.12 eV below the conduction band. However, even without intentional doping, GaN epitaxial layers usually have n-type conductivity with carrier concentration in the 10^{16}-10^{17} cm^{-3} range, caused by Nitrogen vacancies. For p-type doping the acceptor is usually Mg, which resides in the 0.14-0.21 eV range above the valence band. Some basic properties of GaN are summarized in Table 2.1.

Table 2.1: Basic parameters of Gallium Nitride [1].

GaN Parameter	Zinc Blende Structure, Values at 300 K	Wurtzite, Values at 300 K
Density	6.15 g cm^{-3}	6.15 g cm^{-3}
Dielectric Constant	9.7	8.9
Band gap	3.2 eV	3.39 eV
Electron affinity	4.1 eV	4.1 eV
Lattice constant, a	4.52 Å	3.189 Å
Lattice constant, c	Not applicable	5.178 Å

2.1.1 Schottky contacts to GaN

For semiconductors to be used as circuit components, they must make physical and electrical contact with a metal. Electrical contacts can be either of the Schottky or Ohmic type. An Ohmic contact has a linear and symmetric current-voltage characteristic; Schottky contacts rather have a rectifying I-V curve. When the semiconductor and the metal are brought into contact, electrons from the metal diffuse into the semiconductor until thermal equilibrium is established, and the Fermi

levels of the two materials become equal. This causes the bands of the semiconductor to bend, introducing a barrier for further diffusion of carriers. The height of this barrier is determined by the difference between the metal work function, Φ_M, and the electron affinity of the GaN material, χ_{GaN}.

For n-type GaN, the barrier height φ_B is given by $q\varphi_B = q(\Phi_M - \chi_{GaN})$. For p-type GaN, the barrier height expression becomes $q\varphi_B = q\chi_{GaN} + E_G - q\Phi_M$ [20]. Presented on Fig. 2.1 are the barrier heights of Schottky contacts to n-GaN for metals with different work functions [2].

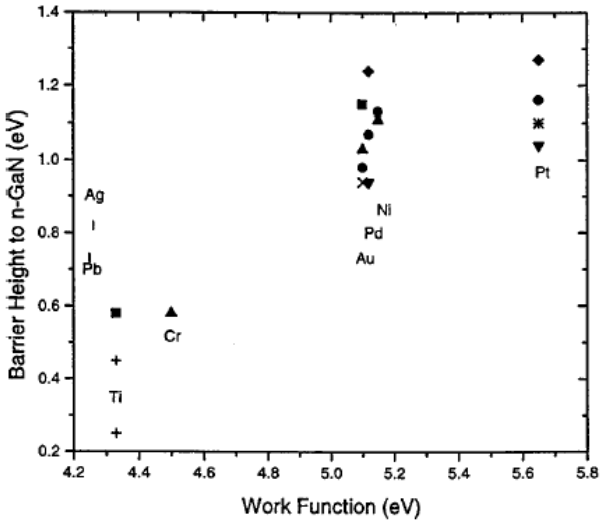

Figure 2.1: Schottky barrier heights on GaN [2, 5–7].

It can be seen that for a good Schottky contact, one would prefer to use a metal that produces a contact with a large barrier height, such as Pt, Ni, Pd, or Au. In practice, Ni is the preferred metal for a Schottky contact due to its high thermal limit of 600 ℃. More recently, good quality Schottky contacts on Cl-treated n-GaN by using a Ni/Au metal stack have been reported [21, 22]. Ni was deposited

first, and each metal was 100 nm thick. An ideality factor n of 1.04 and a barrier height φ_B of 0.95 eV was reported for the Cl-treated n-GaN, as opposed to n=1.16 and φ_B=0.75 eV for the untreated samples. The effective Richardson's constant for GaN was $A^* = 26.4$ A/cm^{2}K^2, as determined by Sawada et. al [23].

Research on the formation of Schottky contacts to p-type GaN depends on the ability to grow high-quality p-type GaN epilayers, which is currently limited. Au has been reported to form a Schottky contact to p-type GaN with a barrier height of 2.38 eV [24].

2.1.2 Ohmic contacts to GaN

From Fig. 2.1, it is also evident that a low barrier height metal, such as Ti or Ag, is preferred for Ohmic contact formation to n-type GaN. From a processing standpoint, Ag is a very problematic metal due to its ease of oxidation. Ti can also oxidize, but when deposited in a thin layer (100-200 Å), followed by a thicker layer of Al, the oxidation on the GaN surface decreases upon annealing.

Traditionally, the choice for an Ohmic metal stack on n-type GaN has been Ti/Al/Ni/Au (Ti deposited first), with metal thicknesses of 200/2000/400/500 Å deposited using e-beam evaporation, and rapid-thermally annealed (RTA) for 30 sec. at 900 ℃. In the literature, specific contact resistivity values for a 900 ℃, 20 s RTA anneal of a Ti/Al stack were reported to be less than 10^{-5} Ω/cm^2 [6]. During annealing, Ti consumes GaN to produce a TiN_x phase, which is in thermodynamic equilibrium with GaN. The role of Al has not been understood completely, but it has

been suggested that the presence of Al reduces the reactivity of Ti with GaN [25]. Without Al, the creation of TiN_x also leads to a large density of vacancies at the Ti/GaN interface. When the contacts are annealed in the presence of Al, $TiAl_3$ limits the creation of TiN_x, fills the voids, and greatly increases the contact reliability.

Tilak has found that optimum surface morphology is achieved with Ti/Al ratio of 0.3, whereas the minimum contact resistance was at a ratio of 0.6 [26]. However, low contact resistance would not be achieved without the Ni/Au layers. While the Au layer provides a pad for electrical probing, the Ni/Au layers prevent oxidation of the underlying Ti/Ai stack, which his essential for achieving low contact resistance. Furthermore, the presence of Ni prevents the diffusion of Au into the Ti/Al stack during annealing. The choice of Ni for this function is not unique, and in fact many other metals have been explored in its place [27]. More recently, V-based metal stacks have been reported as Ohmic contacts to n-AlGaN [28]. Table 2.2 summarizes some recent results Ohmic contact processing to n-GaN and AlGaN/GaN.

Ohmic contacts to p-type GaN are harder to form due to the fact that the sum of the GaN band gap (3.2 eV) and electron affinity (4.1 eV) is greater than the work function of common metals (less than 5 eV). Recently, deposition of 5 nm ZnNi / 380 nm Indium Tin Oxide (ITO) were reported with specific contact resistivity of 1.27×10^{-4} Ωcm^2 [29]. Voss et. al. reported Ohmic contacts to p-GaN using Ni/Au/X/Ti/Au metal stacks, where X is TaN, TiN, or ZrN [30]. Specific contact resistivity as low as 9.0×10^{-6} cm^2 was reported for Ni/Ag/Mg contacts to p-GaN [31]. A plethora of other metals have also been investigated for their contact resistance and reliability and Ohmic contacts to p-type GaN [2].

Year, Group	Contact	Substrate	Results
Mohammed *et al.* [27]	Ti/Au Ti/Mo/Au Ti/Al/Au Ti/Al/metal/Au	AlGaN/GaN AlGaN/GaN AlGaN/GaN AlGaN/GaN	Less rectifying at high T Rc = 0.66 Ωmm, ρ_c = 1.08x10^{-5} Ωcm^2 Rc $\leq$ 0.754 Ω-mm, $\rho_c \leq$ 1.89x10^{-5} Ω/cm^2 Rc $\leq$ 3.2 Ω-mm, $\rho_c \leq$ 1.05x10^{-4} Ω/cm^2
Fernández *et al.* [32]	Ti/Al/Ti-W/Au	n-GaN	Rc = 0.29 Ω-mm
Wang *et al.* [33]	Ti/Al/Mo/Au	AlGaN/GaN n-GaN	Comparable for the two substrates, but different mechanisms of formation
Mohammed *et al.* [34]	Si/Ti/Al/Mo/Au	AlGaN/GaN	Rc $\leq$ 2.0 Ω-mm, $\rho_c \leq$ 1.0x10^{-4} Ω/cm^2
Iucolano *et al.* [35]	Ti/Al/Ni/Au	n-GaN	For 600 ℃ annealing temperature: ρ_c = 3.2x10^{-4} Ω/cm^2 at 300 ℃ ρ_c = 1.75x10^{-4} Ω/cm^2 at 450 ℃ For 800 ℃ annealing temperature: ρ_c = 1.72x10^{-5} Ω/cm^2 at 300 ℃ ρ_c = 8.2x10^{-6} Ω/cm^2 at 450 ℃
Sun *et al.* [36]	Ta/Ti/Al/Ni/Au	GaN/AlGaN/AlN	Rc = 0.16 Ωmm
Hong *et al.* [37]	Ti/Al/Ti/Au	n$^+$ GaN by selective-area growth	Non-annealed contacts ρ_c = 8.9x10^{-5} Ω/cm^2 For 850 ℃ annealing temperature: ρ_c = 1.8x10^{-8} Ω/cm^2
Miller *et al.* [38]	V/Al/V/Au	n-Al$_{0.58}$/Ga$_{0.42}$/N	ρ_c = 4.7x10^{-4} Ω/cm^2
Luther et al. [39]	Al Ti/Al	n-GaN	ρ_c = 8x10^{-6} Ω/cm^2 ρ_c = 5-7x10^{-6} Ω/cm^2

Table 2.2: Comparison of different metallization schemes for Ohmic contacts on n-GaN and AlGaN/GaN structures.

2.1.3 Etching of GaN

GaN can be wet-etched in molten solutions of KOH or NaOH at temperatures above 250 ℃. Even though the etch rates are practical, there are no etch masks to enable etching of GaN for device processing. It is also possible to etch n-type GaN using a photochemical etch process [40–42]. Immersed in KOH at room temperature and UV-illuminated at 365 nm with 50 mW/cm^2 intensity, a 300 nm/min etch rate was obtained. However, the surface roughness and etching profile were not satisfactory for the requirements of modern GaN device processing. In particular, a mesa etch, most commonly employed for device isolation, needs to be deep and with sharp and smooth sidewalls (anisotropic profile), which is best achieves with dry etching processes. The biggest challenge for such etching, however, has been to minimize the plasma-induced damage to the III-nitride.

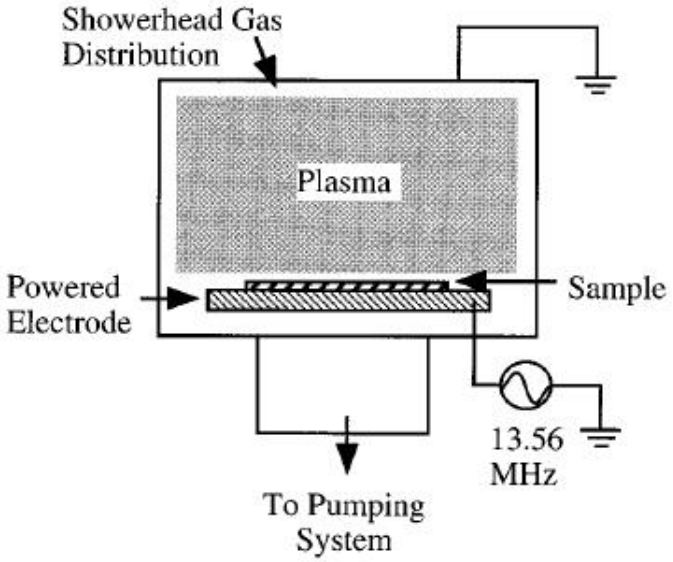

Figure 2.2: Block diagram of an RIE etching system [2].

Figure 2.2 illustrates the principle of operation of a reactive ion etching (RIE) system. Applying an RF frequency signal between two electrodes and supplying a reactive gas between them generates plasma. When the chamber is evacuated to low pressure (up to 200 mTorr), the mean free paths of the ions increase enough to produce an anisotropic etch of the sample. The reactive gas could be $SiCl_4$, which produces an etch rate above 500 Å/min at 400 V DC bias [43]. A more commonly used chemistry involved BCl_3 plasmas, which yielded 1050 Å/min at 150 W cathode RF power [44]. Reports of HBr-, CHF_3-, and CCl_2F_2-based RIE have been published as well [45, 46]. Even though Cl-based RIE resulted in most efficient etching of III-nitride surfaces, the plasma damage resulted in very poor electrical and optical device characteristics. The trade-off was to reduce the etch rate by reducing the ion energy, which gave less anisotropic profiles and limited the critical dimensions. This was especially bad news for RF devices, where the gate-drain and gate-source spacings need to be minimized or the parasitic resistances and capacitances would become too high for RF operation.

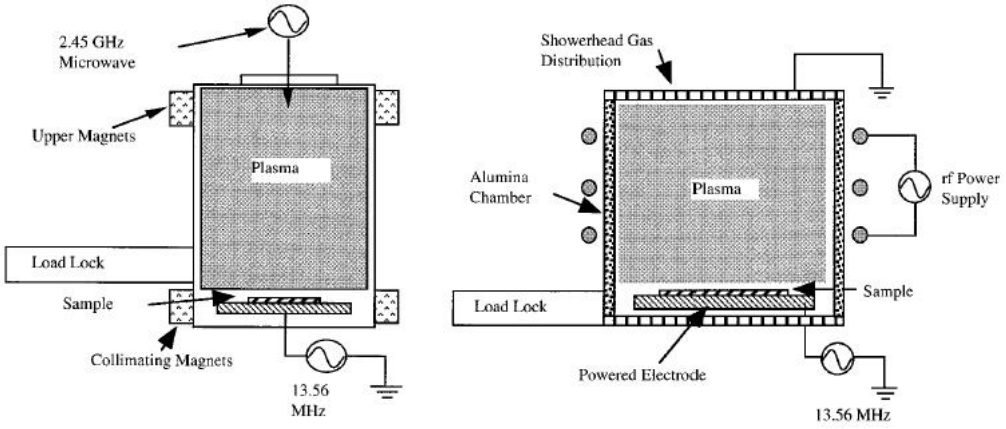

Figure 2.3: Block diagram of an ECR (left) and ICP (right) etching systems [2].

A solution to the problem was found with the development of high-density plasma etching systems. Figure 2.3 shows two possible approaches. The electron cyclotron resonance (ECR) system generates high-density plasma at low pressure (< 5 mTorr) due to magnetic confinement of electrons near the source. The sample is placed downstream, away from the plasma, to reduce the physical damage. Using a Cl_2/H_2 chemistry, Pearton et. al. reported an etch rate of 700 Å/min at 150 V DC bias [47, 48].

Alternatively, an inductively coupled plasma (ICP) is formed by dispensing the plasma chemicals in an insulated chamber and applying RF power through an inductive coil. The resulting magnetic field forces electrons in the center of the chamber and creates high-density plasma there. Thus, the plasma density is separated (decoupled) from the ion energy, and an ICP etch can yield fast etch rates while maintaining low damage to the sample. ICP is advantageous over ECR for its easier and cheaper production-size operation.

Figure 2.4 compares the etch rates obtained using the various dry etching methods described. The reactive ion beam etching (RIBE) method, which reports a similar etch rate to ICP, is performed by generating high-density plasma in a separate source, which is subsequently accelerated to the sample. Figures 2.5–2.7 list the dependence of the etch rate on the pressure, DC bias, and ICP power for the popular $BCl_3/Cl_2/Ar$ chemistry. Figure 2.8 below shows a typical etch profile for such chemistry.

To fabricate a high electron mobility transistor (HEMT), one needs to form Ohmic and Schottky contacts on the AlGaN/GaN structure for contacts, as well

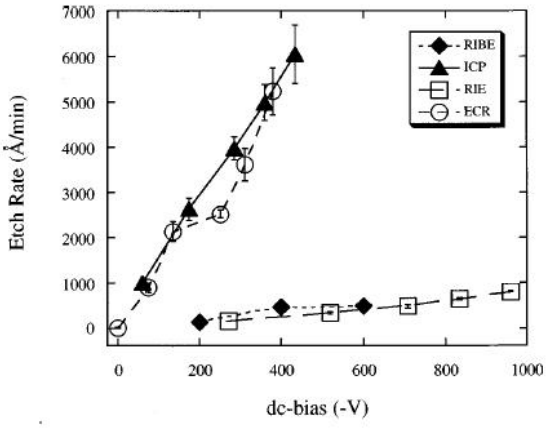

Figure 2.4: GaN etch rates in Cl_2-based plasmas as a function of DC bias [2].

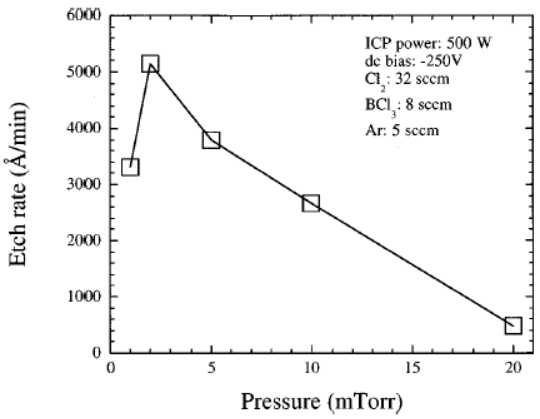

Figure 2.5: GaN etch rates as a function of pressure in BCl_3/Cl_2/Ar ICP plasma [2].

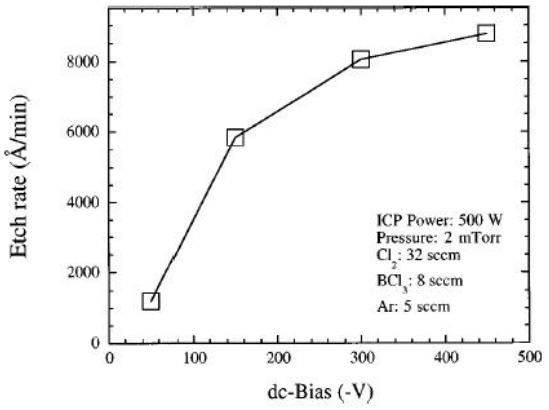

Figure 2.6: GaN etch rates as a function of DC bias in BCl_3/Cl_2/Ar ICP plasma [2].

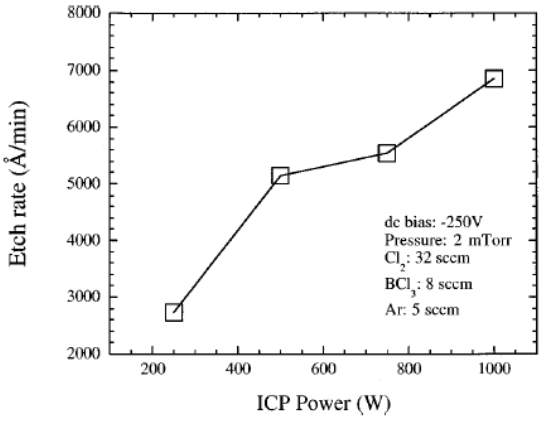

Figure 2.7: GaN etch rates as a function of ICP source power in BCl_3/Cl_2/Ar ICP plasma [2].

as perform a dry etch step for mesa isolation. Now that we have reviewed these processes, we can review the historical literature on HEMT devices.

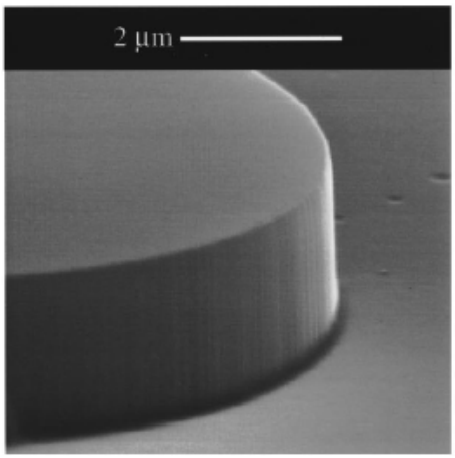

Figure 2.8: Etch profile of GaN etched with ICP under the following conditions: -150 V DC bias, 32 sccm Cl_2, 8 sccm BCl_3, 5 sccm Ar, 500 W ICP source power, 2 mTorr pressure, 10 ℃ electrode temperature [2].

2.1.4 High Electron Mobility Transistors (HEMT)

In 1978, R. Dingle's group at Bell Labs first reported the phenomenon of enhanced electron mobility in modulation-doped semiconductor structures [49]. GaAs and $Al_xGa_{1-x}As$ superlattices were grown using molecular beam epitaxy (MBE), and the modulation doping concept was introduced via an independent Si source. As a result, they were able to spatially separate the mobile electrons from the donors, which caused their existence, thus forming an independent two-dimensional electron gas (2DEG). Such a superlattice structure yielded free electron mobility of the order of 10^4 cm^2/Vs. Even more importantly, this segregation of carriers and impurities caused the material to behave like a metal at low temperatures, where the mobility increased to 1.5x10^4 cm^2/Vs, instead of decreasing as a function of $T^{3/2}$, as the

mobility of a uniformly doped sample would do.

This revolutionary paper was soon followed by a report from Fujitsu by Dr. Mimura [50]. They had reported a GaAs / n-$Al_xGa_{1-x}As$ heterojunction field effect transistor (HFET), a.k.a. high electron mobility transistor (HEMT) using an Al Schottky gate. Hall mobility of 6200 cm^2/Vs at 300 K and 32,500 cm^2/Vs at 77 K was reported, more than five times higher for a MESFET with similar dimensions.

Fundamentally, a HEMT is not very different from a MOS transistor. Instead of the low quality GaAs native oxide on top of the material hosting the conducting channel (Fig. 2.9a), we grow a modulation-doped semiconductor layer (in the above case, $Al_xGa_{1-x}As$), in order to achieve the carrier confinement below the Fermi level near the interface (Fig. 2.9b).

High mobility alone was not enough for GaAs-based HEMT devices to make a breakthrough among high-frequency devices. In principle, lower mobility can be compensated with larger device dimensions if switching speed was not an issue. But due to the capability of GaAs to form semi-insulating substrates, the capacitance underneath the source/drain regions (bottom capacitance) was eliminated, which significantly reduced the source-substrate (Csb) and drain-substrate (Cdb) capacitances, which in turn enabled faster switching. Another advantage of the semi-insulating technology was easier device isolation, which contributed to the reduced circuit size. There were several major disadvantages of GaAs technology, however.

First, the native oxide had very low quality, as we mentioned, and MOS technology was not viable. The usage of Schottky metals for a gate meant higher gate

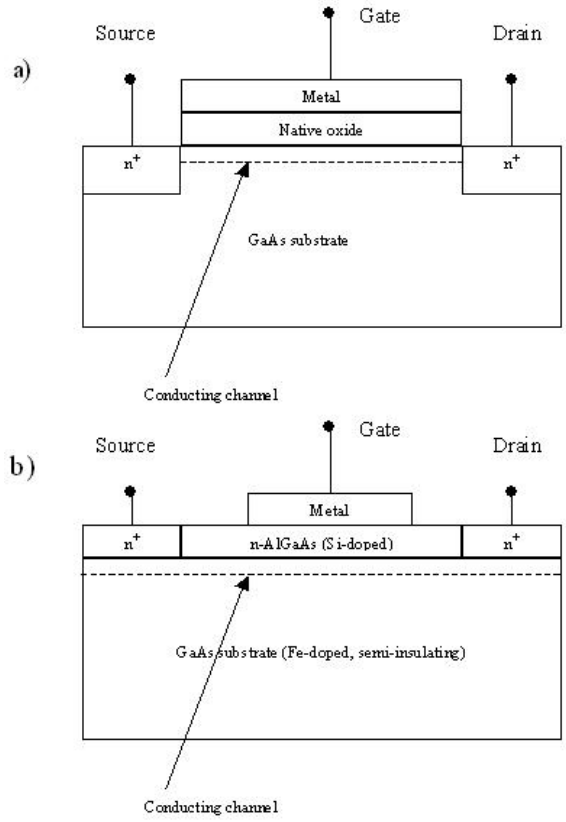

Figure 2.9: (a) GaAs-based MESFET, (b) GaAs-based HEMT.

leakage and higher density of interface states, which degraded device performance. Also, CMOS technology was not an option since p-type GaAs had hole mobility of about 10 cm^2/Vs. Finally, the presence of a conducting channel at zero gate bias meant that circuits had to be designed with depletion-mode devices only, which increased the power consumption of the HEMT-based circuits.

Despite their shortcomings, GaAs HEMT devices found immediate application in high-frequency circuits such as satellite receivers, enabling a revolution in the penetration of satellite television in Japanese households, for example.

Even though GaN was known as a material since 1938, it was first epitaxially

grown in 1969 by HVPE by Maruska and Tietjen at RCA labs [51]. During the early 1970's, efforts to grow GaN by MBE and MOCVD were successful, but p^+ type doping of GaN, essential for the production of blue LEDs, remained elusive. For the next 15 years or so, people were trying unsuccessfully to understand the physics of p-type doping in GaN, until Nakamura, working quietly in his lab at Nichia, was able to do it in 1991 [52]. His succeeded by removing all Hydrogen from the growth chamber, which was later shown to passivate the acceptor sites. Following the success of GaN LED devices, in 1992 III-nitride materials were proven viable for HEMT devices with the demonstration of a 2DEG in GaN by Khan et. al., and the demonstration of an AlGaN/GaN HEMT by the same group the following year [53, 54]. Another milestone was achieved when Binari et. al. demonstrated the operation of insulated-gate GaN devices [55, 56]. Table 2.3 lists the historical development of GaN-based transistors.

When GaN is grown on sapphire or SiC, it forms the wurtzite crystal structure, which is non-symmetric, and leads to a strained interface and a piezoelectric induced charge in AlGaN/GaN heterostructures [57]. III-nitrides are more ionic in nature than III-V materials. Therefore, according to Yu and Martin, the dipole moment arising from the displacement from the atomic core increases relative to the strain-induced changes in charge distribution along the bond direction and within the atomic cores [58, 59]. Figure 2.10 shows calculated and measured sheet charge concentrations for $Al_xGa_{1-x}N$/GaN heterostructures as a function of the Al mole fraction.

The high carrier density in the 2DEG for the AlGaN/GaN structure has lead to

Table 2.3: Historical Development of GaN electronics [2, 3].

Year	Event	Authors
1969	GaN by hydride vapor phase epitaxy	Maruska and Tietjen
1971	MIS LEDs	Pankove *et al.*
	GaN by MOCVD	Manasevit *et al.*
1974	GaN by MBE	Akasaki and Hayashi
1983	AlN intermediate layer by MBE	Yoshida *et al.*
1986	Specular films using AlN buffer	Amano *et al.*
1989	*p*-type Mg-doped GaN by LEEBI and GaN *p-n* junction LED	Amano *et al.*
1991	GaN buffer layer by MOCVD	Nakamura
1992	Mg activation by thermal annealing	Nakamura *et al.*
	AlGaN/GaN two-dimensional electron gas	Khan *et al.*
1993	GaN MESFET	Khan *et al.*
	AlGaN/GaN HEMT	Khan *et al.*
	Theoretical prediction of piezoelectric effect in AlGaN/GaN	Bykhovski *et al.*
1994	InGaN/AlGaN DH blue LEDs (1 cd)	Nakamura *et al.*
	Microwave GaN MESFET	Binari *et al.*
	Microwave IIFET, MISFET	Binari *et al.*; Khan *et al.*
	GaN/SiC HBT	Pankove *et al.*
1995	AlGaN/GaN HEMT by MBE	Ozgur *et al.*
1996	Doped channel AlGaN/GaN HEMT	Khan *et al.*
	Ion-implanted GaN JFET	Zolper *et al.*
	340 V V_{GD} AlGaN/GaN HEMT	Wu *et al.*
	1st blue laser diode	Nakamura and Fosal
1997	Quantification of piezoelectric effect	Asbeck *et al.*
	AlGaN/GaN HEMT on SIC	Binari *et al.*; Ping *et al.* Gaska *et al.*
	1.4 W @ 4 GHz	Thibeault *et al.*
	0.85 W @ 10 GHz	Siram *et al.*
	3.1 W/mm at 18 GHz	Wu *et al.*
1998	3.3 W @ 10 GHz	Sullivan *et al.*
	p/n junction in LEO GaN	Kozodoy *et al.*
	HEMT in LEO GaN	Mishra *et al.*
	6.8 W/mm (4 W) @ 10 GHz HEMT on SiC	Sheppard *et al.*
	10^{-4} Hooge factor for HEMT on SiC	Levinshtein *et al.*
	1st AlGaN/GaN HBT	McCarthy *et al.* Ren *et al.*
	1st GaN MOSFET	Ren *et al.*

very high mobility results as well. Shur et. al. reported the theoretical effects on the mobility due to ionized impurity scattering, polar optical scattering, piezoelectric scattering, and acoustic scattering [8]. Figure 2.11 shows their results, with polar optical scattering dominating at high temperatures, whereas piezoelectric scattering

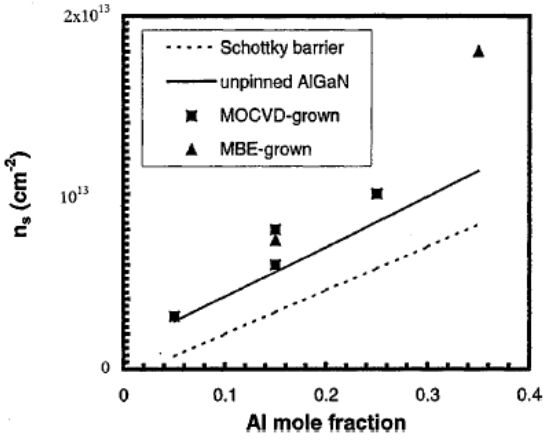

Figure 2.10: Sheet electron density vs. Al mole fraction for undoped $Al_xGa_{1-x}N$/GaN HEMT structures. Dots indicate Hall measurements, whereas lines indicate calculated density using a Schottky contact to the AlGaN surface [8].

dominant at low temperatures.

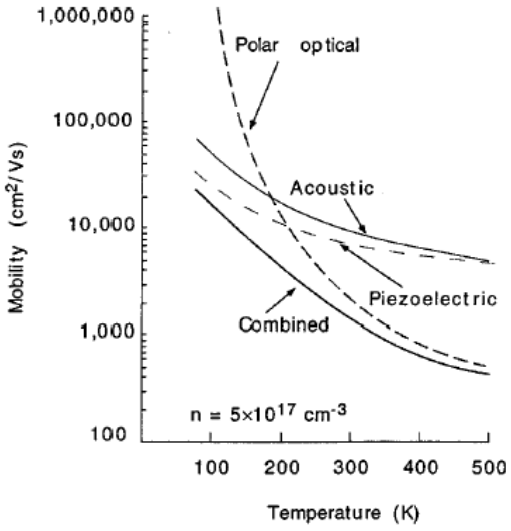

Figure 2.11: Electron mobility in a HEMT 2DEG due to polar optical, acoustic, and piezoelectric scattering as a function of temperature [8].

For an AlGaN/GaN HEMT grown on 6H-SiC, Shur's group also measured

mobility of 2000 cm^2/Vs and sheet carrier density of 1.3x10^{13} cm^{-2} at 300 K. The mobility increased to 10250 cm^2/Vs at 10 K [60].

Figure 2.12 shows the quantified effect of ionized impurity scattering on the mobility of GaN. The total impurity concentration was 7.5x1016 cm^{-3}, and the carrier densities were 5x10^{17} cm^{-3} (curve 1), 2x10^{17} cm^{-3} (curve 2), 7.5x10^{16} cm^{-3} (curve 3), and 2x10^{16} cm^{-3} (curve 4).

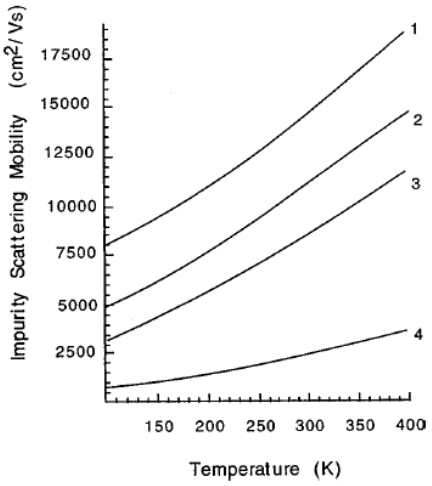

Figure 2.12: Impurity scattering mobility vs. temperature and sheet carrier density in an AlGaN/GaN HEMT electron gas [8].

Among the topics in the recent HEMT research, three categories stand out. First and foremost has been the task of reducing the current collapse phenomenon, which has been directly related to the surface passivation of the AlGaN layer. This has also necessitated research into the choice of passivation dielectrics. Secondly, the breakdown voltage of HEMT devices has been increasing with the usage of field plate techniques for spreading the gate-drain electric field. Thirdly, self-heating effects have been limited by using lower current ratings, lower switching frequency,

and pulsed-mode operation. In addition, enhancement mode normally-off operation has been sought for GaN HEMT and FET devices, in order to make them more competitive in their quest for commercialization. The following sections detail recent literature in each category.

More recently, AlGaN/GaN HEMT devices were explored to correlate their DC characteristics with SiC substrate micropipe defects [61], and even fabrication on plastic substrates for flexible circuit applications [62]. The Pearton/Ren group has also demonstrated the use of AlGaN/GaN HEMT as detectors for hydrogen [63] and prostate cancer specific antigens (PSA) [64]. This research may have a far-reaching influence since prostate cancer accounts for 10 % of all cancer deaths in the United States.

2.1.5 Surface passivation and current collapse

An excellent overview of current collapse (a.k.a, RF dispersion, current compression, and current slump) was published by Vetury et al. [9]. Suppose that, due to poor surface passivation, negative charge traps on or near the surface of an AlGaN/GaN HEMT. This charge would repel some electrons from the 2DEG, this extending the depletion region under the gate (Fig. 2.13a). As a result, the surface-trapped charge acts like a negatively charged metal gate, and has been referred by Vetury as a "virtual gate," or V_{VG}. The virtual gate will be in series with the gate of the device, and will thus control the drain current as well (Fig. 2.13b).

The band diagram of the device changes accordingly, as shown below.

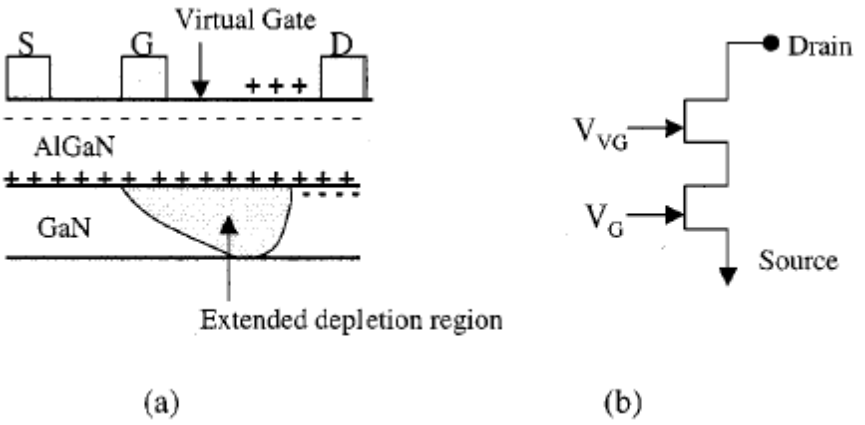

Figure 2.13: (a) Extended depletion region of an AlGaN/GaN HEMT due to the presence of a virtual gate, resulting in an equivalent circuit (b) [9].

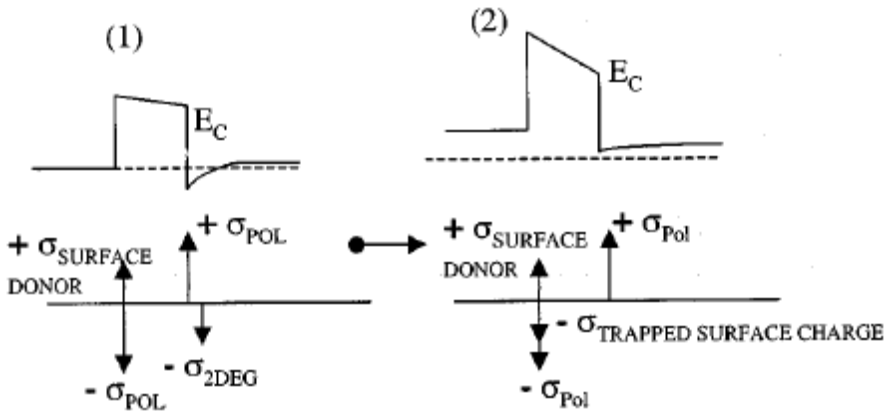

Figure 2.14: Energy band diagram and charge distribution of an AlGaN/GaN HEMT without (1) and with (2) trapped negative surface charge [9].

Therefore, as V_G increases, so will V_{VG}, and the drain current will decrease. The magnitude of V_{VG} also depends on the frequency of V_G because the time constant associated with trapping and detrapping of electrons near the gate is smaller that the device operating frequency. In other words, if V_G is an AC signal, the traps

are fast enough to fill and empty and the magnitude of V_G changes.

As pointed out by Koudumov et. al., the best way to solve the current collapse problem in the long term is to improve the material and substrate quality [65]. A major problem is the presence of threading dislocations in epitaxial III-nitride materials. Even though research in developing GaN native substrates has made very good progress in recent years, there are still no commercial GaN substrates available. Therefore, current short-term solutions focus on reducing surface trap density, for which the AlGaN device surface needs to be well passivated. This will also decrease surface leakage and increase contact reliability.

There have been numerous reports of passivation of AlGaN surfaces by deposition of SiN_x [10, 66–69]. Figure 2.15 shows the current-voltage characteristics of a non-passivated and a SiN_x-passivated Schottky diodes. The reverse leakage was reduced by 2.5 orders of magnitude by performing the SiN_x passivation step.

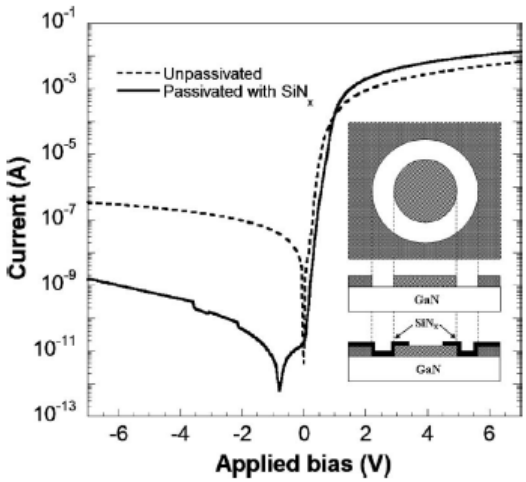

Figure 2.15: Reduction in Schottky diode reverse leakage by SiN_x passivation [10].

On Fig. 2.15, the SiN_x deposition was performed *ex situ* by remote plasma

enhanced CVD at 300 ℃ for a thickness of approximately 10 nm. An even more-effective passivation has been achieved by performing the SiN_x growth *in situ*, i.e., immediately after the AlGaN/GaN layers are grown, while the sample is still in the reactor [70, 71].

2.1.6 High breakdown voltage design

The two most important parameters in power switching device design are the breakdown voltage and the on-state resistance of the device. For lateral HEMT devices, the on-state resistance (a.k.a., on-resistance) is given by Equation 2.1:

$$R_{ON} = \frac{4V_{BR}^2}{\epsilon_r \mu_n E_{C_{GaN}}^3} \tag{2.1}$$

given in units of mΩ-cm^2, where ϵ_r is the dielectric constant, μ_n is the mobility, V_{BR} is the breakdown voltage, and $E_{C,GaN}$ = 3.3x10^6 V/cm is the critical breakdown field of GaN. For comparison, the critical breakdown field of GaAs is only 0.4x10^6 V/cm [72]. Figure 2.16 shows the theoretical limits of the on resistance as a function of the breakdown voltage for Si, SiC, and GaN, calculated using Equation 2.1.

The relationship V_{BR}^2 / R_{ON} is one figure of merit (FOM) for the device. Due to high electron density and high mobility of the 2DEG, AlGaN/GaN HEMT devices typically have around two orders of magnitude lower on resistance than their SiC counterparts.

Even though the wide bandgap of the III-nitride materials gives them inher-

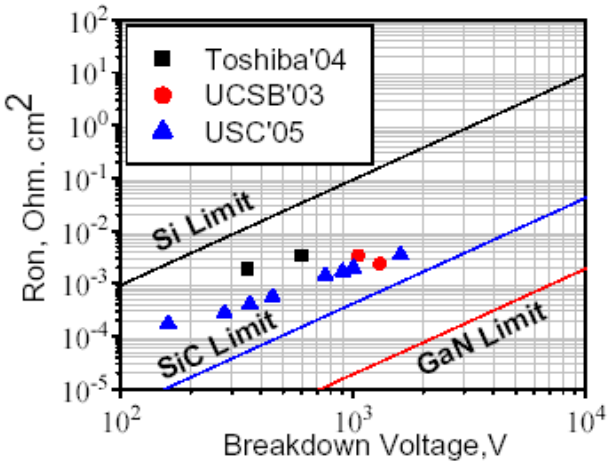

Figure 2.16: Theoretical R_{ON} vs. V_{BR} for Si, SiC, and GaN [11].

ently high breakdown voltage, a device can be designed for high breakdown voltage as well. The most important method involves the concept of a field plate, which is nothing more than an extension of either the source or the drain metal to cover a portion of the device channel. By doing so, the electric field peak in the channel is reduced, and the overall breakdown voltage is increased. Most importantly, field plates help suppress surface trapping and thus current collapse phenomena [73].

By using such techniques, AlGaN/GaN HEMT devices with breakdown voltage of 1.6 kV and on-resistance of 3.4 mΩ cm^2 were demonstrated recently. The breakdown voltage depended linearly on the gate-drain spacing (L_{GD} = 6 μm resulted in V_{BR} = 200 V, L_{GD} = 20 μm gave V_{BR} = 1600 V).

A field plate could be fabricated by extending either the source [74] or the gate metallization, or by employing a floating gate approach [62]. Multiple field plates could also be utilized for even better performance [75].

Most recently, the design of an $Al_xGa_{1-x}N/Al_yGa_{1-y}N$/AlN HEMT with 1650 kV

breakdown voltage for L_{GD} = 10 μm was demonstrated without any field plate design [72]. This very encouraging result was achieved with x=0.53 and y=0.38 Al mole fractions, and a Si implantation (annealed at 1200 ℃ for 5 min) underneath the source/drain regions.

2.1.7 Self-heating effects

Self-heating occurs in transistors due to when channel electrons with high energy (hot electrons) transfer energy to the lattice, and thus heat up the device [76]. For HEMTs, self-heating has been particularly significant when the device was fabricated on a substrate with low thermal conductivity (k) such as semi-insulating GaAs ($k_{semi-insulatingGaAs}$ = 0.51 W cm^{-1} K^{-1} at 305 K) or sapphire ($k_{sapphire}$ = 0.351 W cm^{-1} K^{-1}) [77]. Figure 2.17 shows the channel temperature as a function of the dissipated power when a sapphire substrate is used instead of Si (k = 1.422 W cm^{-1} K^{-1} at 300 K) [78].

As the channel temperature increases, phonon scattering phenomena in the lattice occur more rapidly, causing carrier mobility in the channel to decrease. This leads to an increase in the source resistance, and thus a decrease in the source-drain current. A negative differential resistance effect is thus introduced and is present during high power dissipation. Gaska et. al. reported a decrease in the HEMT thermal impedance, Θ, of more than an order of magnitude (from Θ = 25 ℃ mm-W^{-1} down to Θ = 2 ℃ mm-W^{-1}) when a 6H-SiC substrate was used instead of sapphire [79]. This reduction translated directly into an increase of drain voltage

required to achieve the same reduction in drain current. For the HEMT on a sapphire substrate, reducing Ids by 10 % required a ΔVds of 6 V (from 7 V to 13 V). When the substrate was SiC (approximately 10 times larger thermal conductivity), ΔVds required to achieve the same 10 % reduction in drain current was 30 V (from 10 V to 40 V).

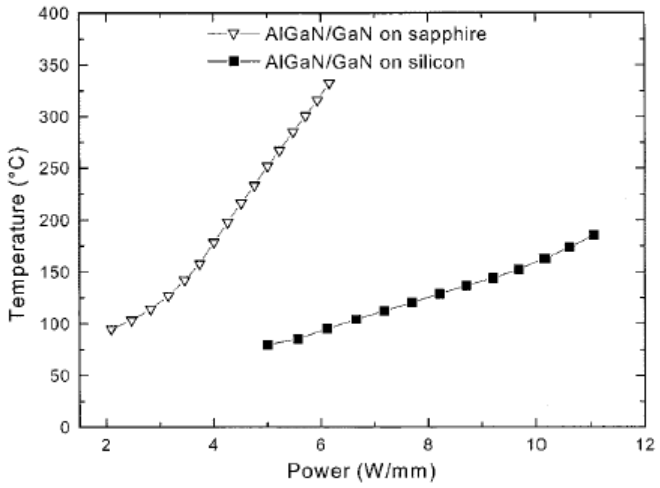

Figure 2.17: HEMT channel temperature vs. dissipated power for sapphire and Si substrates [12].

On Fig. 2.17, the channel temperature was not directly measured, but set approximately using an external heater. This measurement was then used as a calibration for extracting the HEMT channel temperature form the Raman signal (Fig. 2.18). [13]

To avoid self-heating problems, pulsed current measurements have been generally employed in the literature. Publications that have addressed self-heating have provided insight by characterization [80] and modeling [81–84].

Apart from choosing higher thermal conductivity substrates, a topside dia-

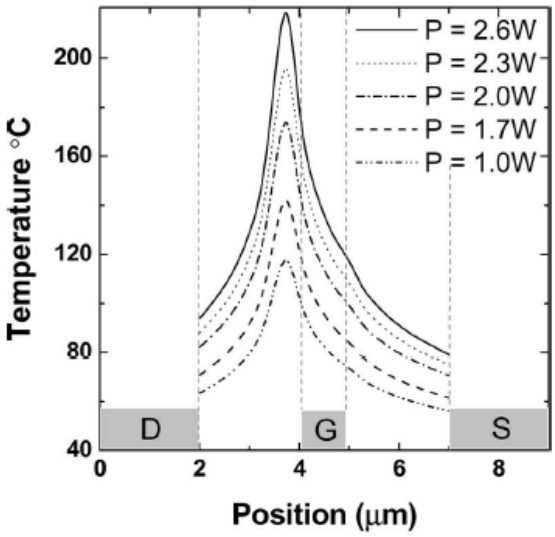

Figure 2.18: Temperature profile in AlGaN/GaN HEMT channel measured by Raman spectroscopy [13].

mond cap has been attempted by Seelman-Eggebert et al. [85]. The main problem of their approach was the thermal damage caused to the device by the high temperature of diamond deposition. Our solution to this problem is presented in the next chapter.

2.1.8 Normally-off operation

The quest to make AlGaN/GaN HEMT devices more accessible to traditional circuit design methods has necessitated research into normally off device operation. In reality, the biggest problem with normally on devices is if, for some reason, all device gates become grounded. This would result in connecting the power applied to all drains to the grounded sources, thus shorting the external power supply and causing unsafe operation. Enhancement mode (normally off) devices provide a fail-

safe during circuit power interruption.

Mizutani et. al. utilized the polarization field of a 5 nm thick $In_{0.2}Ga_{0.8}N$ cap layer grown on top of the traditional AlGaN/GaN structure [86]. The threshold voltage shifted from -1.5 V to +0.4 V when devices with and without the $In_{0.2}Ga_{0.8}N$ layer were compared. A similar effect was achieved by depositing a 2 nm thick SiN_x layer on AlN/GaN devices, causing it to induce a 2DEG in the HEMT. However, this method led to poor mobility results (approximately 200 cm^2/Vs).

Song et. al. achieved normally-off operation by implanting negatively-charged F ions in the region directly underneath the HEMT gate [87]. Therefore, when the gate bias was removed, the negative charge would repel the 2DEG electrons underneath the gate, effectively removing the continuous presence of electrons in the channel and turning off the device. The advantage of this approach is that it affects the breakdown voltage similarly to a field plate, but does not introduce any parasitic capacitances. The method also reduced the current collapse in the device without affecting the cutoff frequency or the gain.

Recently, normally off operation of AlGaN/GaN based HEMTs was demonstrated using an AlGaN-selective wet etch approach by Anderson et al. [88]. This novel process is the topic of Section 2.3.2.

2.2 Fabrication of AlGaN/GaN HEMT Devices

In this section, we present our standard HEMT processing sequence, along with process optimization experiments. A description of HEMT fabrication sequences is given in Chapters 3 and 4 for the relevant structures presented there. Appendix III gives the complete process sheets for HEMT device fabrication.

HEMT devices were typically fabricated on a 25 nm AlGaN / 2 μm GaN HEMT structures, grown on a-plane sapphire substrates. The sample was initially cleaned in an SC-1 solution (more details are given below). Device isolation was performed by etching mesas using a Cl-based ICP etch process. This step can be performed either first or last in the process sequence. Following Ohmic contact patterning, the sample was ashed and cleaned again, and Ti/Al/Pt/Au contacts were deposited using e-beam evaporation. Contact annealing was performed at 900 ℃ for 30 seconds in flowing N_2. Ni/Au layers were deposted for gates, and a passivation layer of SiN_x was deposited. Contact windows were etched in the nitride using SF_6 chemistry and a second metal stack of Ti/Pt/Au was deposited for probing pads. The resulting current-voltage characteristics are presented in Fig. 2.19, and some device parameters are given in Table 2.4.

Once a functional HEMT device was obtained, several studies were peformed to optimize several key device parameters. Sheet resistance, mobility, and carrier density largely depended on the quality of the material obtained. Studies of cleaning procedures, choice of contact metals, and contact annealing conditions were employed to reduce the contact resistance and thus the on resistance. The propri-

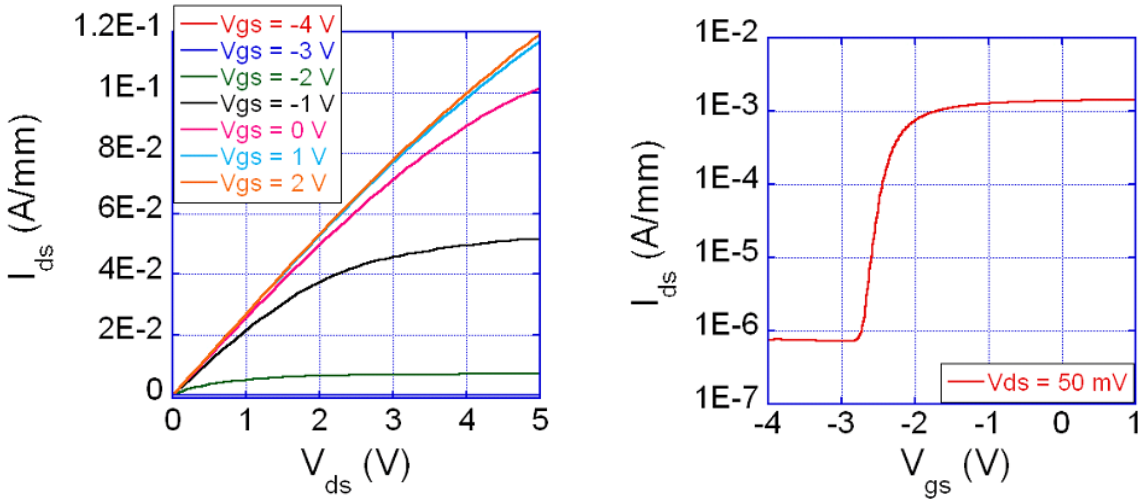

Figure 2.19: Current-voltage characteristics of a typical HEMT sample.

Table 2.4: Typical devices parameters obtained from a standard HEMT.

Device Parameter	NRL HEMT	Commercial HEMT
Hall Probe R_{SH} (Ω/sq.)	1460	513
Hall Probe μ_h (cm^2/V-s)	1193	1527
Hall Probe N_{SH} (cm^{-2})	$3.9x10^{12}$	$8.35x10^{12}$
TLM R_{SH} (Ω/sq.)	1217.61	557
TLM R_C (Ω-mm)	1.76	0.309
ρ_c (Ω-cm^2)	$2.54x10^{-5}$	$1.7x10^{-6}$
V_T (V)	-2.75	-2.22
I_{DSS}, V_{GS} = 2 V (A/mm)	0.12	0.143
$G_{m,MAX}$ (S/mm)	$1.66x10^{-3}$	0.153
I_{ISO} (A/mm), V_{DS} = 10 V	$2x10^{-6}$	$1.8x10^{-9}$
R_{ON} (Ω-mm)	36.8	14.7
Φ_B (eV)	0.939	0.66
Ideality Factor, n	1.34	0.99

etary GaN nucleation layer of the commercial wafers contributed to the three orders of magnitude lower buffer isolation current I_{ISO}. The buffer leakage in the NRL

HEMT material could also be high because the reactor was not devoted exclusively to undoped GaN growth, and thus the unintentional Si doping could have been significant. This fact could have lead to a higher defect density as well, leading to reduced mobility and sheet carrier density.

One of the biggest concerns during fabrication is sample cleanliness. Special care must be taken to avoid sample contamination with metallic and organic particles, as well as unnecessary oxidation. Several standard methods have been developed in the past, most notably at Radio Corporation of America Labs (RCA), where the SC-1 and SC-2 methods were developed.

Standard cleaning solution no. 1 (SC-1) consists of a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and DI water (H_2O). A typical concentration ratio for the mix is 1:1:5 NH_4OH:H_2O_2:H_2O. The SC-1 solution is the best known treatment for removing particles from the surface of the wafer. The SC-1 solution is also very effective at removing organic contaminants and some metallic contaminants. Standard cleaning solution no. 2 (SC-2) consists of a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2), and DI water (H_2O). A typical concentration ratio for the mix is 1:1:5 HCl:H_2O_2:H_2O. The SC-2 solution is best for removing metal contaminants from the wafer surface, and it usually follows the SC-1 in the cleaning sequence. The two solutions clean by continually oxidizing and then etching the surface of the wafer, thereby dissolving the contaminants. We used the solutions at temperature of around 60 ℃, though a range of 50-70 ℃is common.

The SC-1 and SC-2 solutions described above are typically to clean samples prior to fabrication. At intermediate steps, especially prior to creating interfaces

with oxides or metals, cleaning procedures are used to remove any native oxide that may have formed on the sample surface. GaN-based devices are usually cleaned in dilute solutions of HCl or NH_4OH, usually in 1:10 ratio with DI water for up to 1 minute. This time is usually shorter for NH_4OH, especially if a patterned sample is being cleaned (NH_4OH develops resist).

Table 2.5 presents a combination the above cleaning methods on six samples. The SC-1 and SC-2 cleans were employed on the wafers prior to fabrication. The samples were then patterned for Ohmic contacts, and cleaned in dilute HCl or NH_4OH. After Ohmic contact formation, the sheet and contact resistance was measured and reported below.

Table 2.5: Comparison of wafer cleaning methods prior to device fabrication.

	R_{SH} (Ω/sq.)	R_C (Ω-mm)	ρ_C (Ω-cm^2)
Solvent Clean, HCl	1398	1.28	1.1x10^{-5}
Solvent Clean, NH_4OH	979	0.6629	4.5x10^{-6}
SC-1 Clean, HCl	1511	1.556	1.6x10^{-5}
SC-1 Clean, NH_4OH	1588	1.683	1.8x10^{-5}
SC-1+SC-2 Clean, HCl	1289	1.395	1.5x10^{-5}
SC-1+SC-2 Clean, NH_4OH	1868	1.162	7.2x10^{-4}

Current-voltage measurements were performed on the gateless HEMT devices, with results summarized in Fig. 2.20.

Next, different Ohmic contact metallization stacks were compared. In the literature review, we described a plethora of metal combinations. Here we chose a traditional Ti-based contact, but we varied the barrier metal among Ni, Ti, and Pt. The metal thicknesses were 20 nm Ti, 80 nm Al, 40 nm Ni/Ti/Pt, and 50 nm Au,

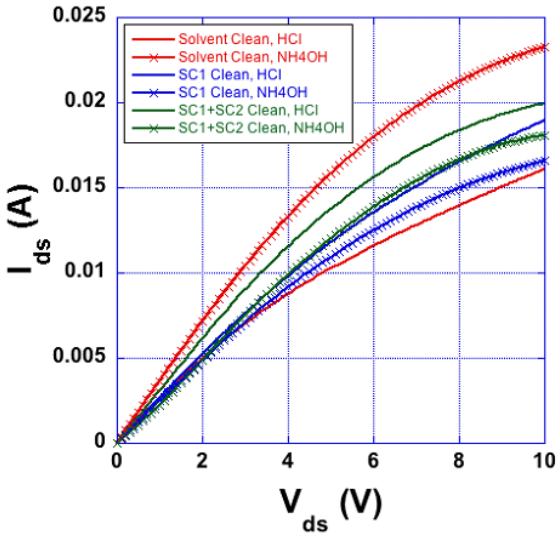

Figure 2.20: Current-voltage characteristics of devices cleaned using different methods.

deposited by e-beam evaporation. The annealing time was 30 sec. at temperatures between 750 ℃ and 900 ℃. The results are presented in Table 2.6, where the reported numbers are the sheet resistance, contact resistance, and specific contact resistivity.

Regardless of the barrier metal used, the best performance was obtained at 850 ℃. Contacts based on the Ti/Al/Ti/Au stack exhibited the lowest sheet and contact resistances. The main reason Ti/Al/Pt/Au contacts gave the highest contact resistance was the high temperature of Pt deposition, which made subsequent lift-off harder. This was especially true for gate metals, where Ni/Au gave much more reliable results. Ohmic contact resistance was further optimized by increasing the thickness of the Al layer and performing an HCl dip prior to evaporation. Specific contact resistivities in the low 10^{-6} Ω-cm^2 range have been routinely obtained with a 2 minute 10 W O_2 plasma ash followed by a 30 sec. dilute HCl dip, and a 120 nm Al

Table 2.6: Comparison of Ohmic contact metallization and annealing schemes. All samples were rapid-thermal annealed for 30 seconds. Reported values, in column order, are sheet resistance R_{SH} ($\Omega/sq.$), contact resistance R_C (Ω-mm), and specific contact resistivity ρ_c (Ω-cm^2).

Metals	Annealing temperatures			
	750 ℃	800 ℃	850 ℃	900 ℃
Ti/Al/Ni/Au	2730 7.00 $1.8\text{x}10^{-4}$	2435.3 2.51 $2.58\text{x}10^{-5}$	1907.8 0.45 $1.08\text{x}10^{-6}$	1993.8 3.17 $5.05\text{x}10^{-5}$
Ti/Al/Pt/Au	4026.5 11.84 $3.48\text{x}10^{-4}$	785085.6 N/A N/A	1537.12 8.68 $4.9\text{x}10^{-4}$	27968.72 409.73 $6.0\text{x}10^{-2}$
Ti/Al/Ti/Au	1032.13 5.99 $3.48\text{x}10^{-4}$	1305.93 18.17 $2.53\text{x}10^{-3}$	842.4 0.53 $3.38\text{x}10^{-6}$	1695.72 N/A N/A

thickness in the Ti/Al/Ni/Au stack. It must be noted, however, that these results were highly dependent on the deposition equipment, metal quality, and process variables such as soak time and power. Therefore, the process should be tuned by the engineer as results will vary.

One of the most important parameters for power switching devices is the breakdown voltage. We characterized our HEMT devices using a pulsed drain bias up to 1000 V, supplied by a Keithley 237 source-measurement unit. The duty cycle was 10 %, and the device was biased in the off state with $V_{GS} < V_T$. A breakdown voltage of about 750 V was measured on a device with a 15 μm gate to drain spacing (Fig. 2.21). Although some high voltage testing resulted in catastrophic breakdown, typically stressed devices exhibited increased reverse gate leakage current, as shown in Fig. 2.22.

The off-state current at $V_{DS} < V_{BR}$ was found to be highly dependent on

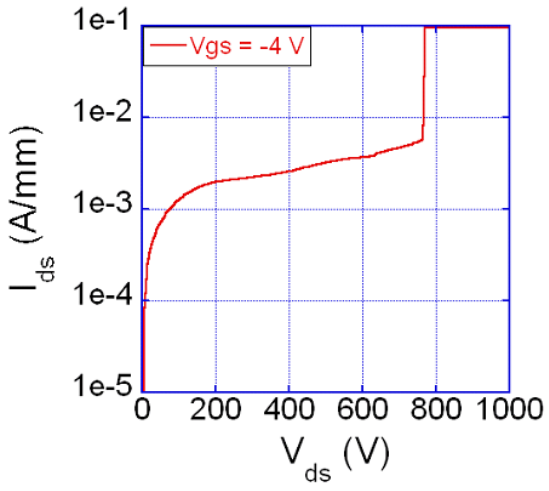

Figure 2.21: Forward blocking mode breakdown voltage characteristics of a typical HEMT.

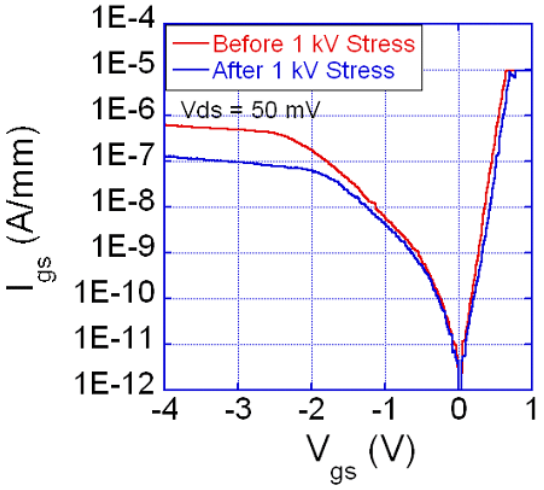

Figure 2.22: I_{GS}-V_{GS} characteristics before and after breakdown voltage measurement.

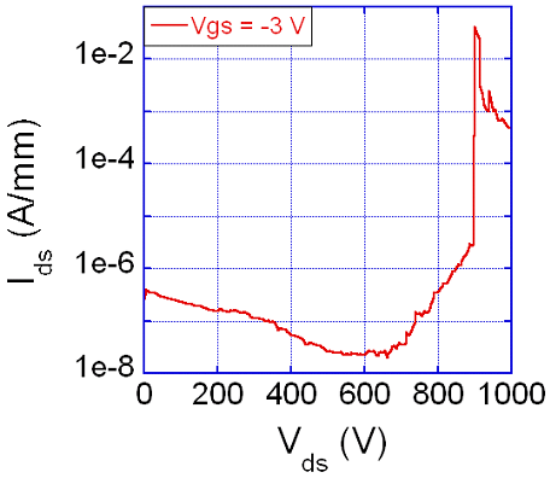

Figure 2.23: Breakdown voltage characteristics of a low buffer leakage HEMT.

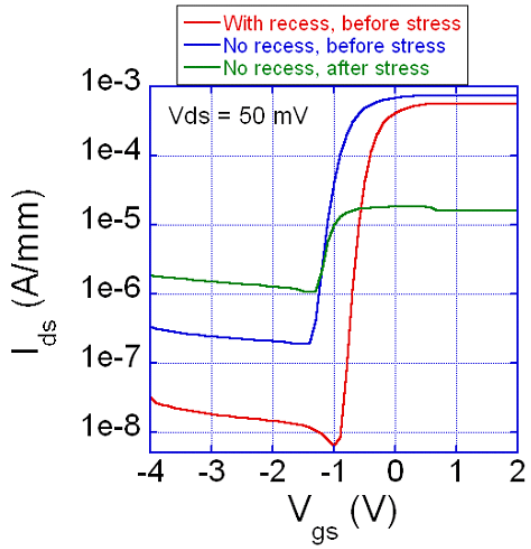

Figure 2.24: I_{DS}-V_{GS} characteristics of the low buffer leakage HEMT before and after stress.

the leakage in the AlN buffer layer. Buffer leakage (a.k.a. device isolation current) was measured between adjacent devices and was could vary up to four orders of magnitude. Figure 2.23 shows that reduced buffer leakage leads not only to low off state current, but also to a higher breakdown voltage (about 900 V in this case). Figure 2.24 shows the I_{DS}-V_{GS} characteristics before and after stress, highlighting the increased off state current after breakdown stressing. The plot also shows breakdown voltage data for devices without a gate recess. For comparison, the I_{DS}-V_{GS} characteristic of a recessed gate HEMT is shown to emphasize the further reduction in off state leakage obtained using that approach. More details on recessed-gate HEMTs will be provided in the next section.

2.3 Enhancement Mode HEMT Devices

This section presents the results of fabricated HEMT devices with thinned AlGaN regions. This approach has been extensively pursued in the past as a method of obtaining enhancement mode devices [14, 89–92]. Figure 2.25 shows a linear relationship between HEMT threshold voltage and the thickness of the AlGaN layer. The increase in threshold voltage is achieved by reducing the sheet carrier density, which makes the channel easier to deplete, which means that less negative gate bias needs to be applied to create a depletion region underneath the gate.

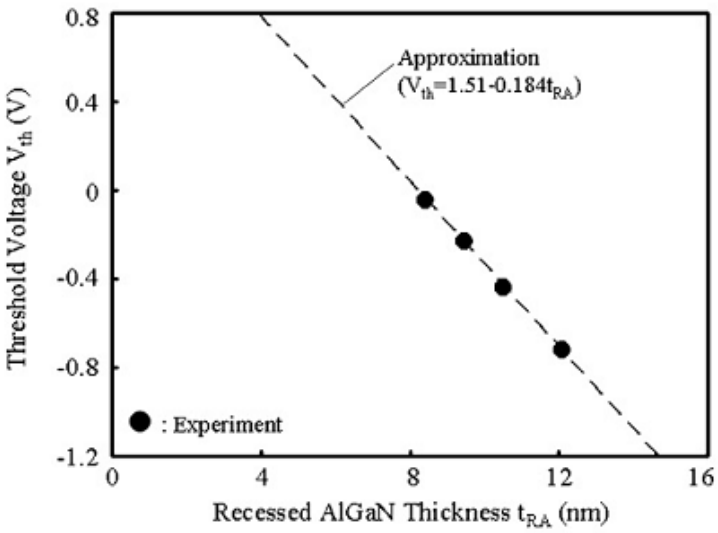

Figure 2.25: Dependence of AlGaN/GaN HEMT threshold voltage on the thickness of the AlGaN layer underneath the gate [14].

Reducing the sheet carrier density, and thus the threshold voltage, by employing thin AlGaN layers has the major drawback of increasing the on-state resistance of the device. For this reason, thinning the AlGaN layer is only performed beneath

the gate, most commonly by dry etching. Another drawback is the etch damage caused by the dry etch which leads to unstable gate characteristics. The opposite approach of growing a thin AlGaN layer creates high resistance throughout the channel, which is an even less attractive option. In this section, we present our results from thinning the AlGaN layer using ICP etching.

2.3.1 AlGaN/GaN HEMT devices with dry etched gate recess area

The AlGaN/GaN HEMTs studied in this section were similar to the ones presented in the previous section. The Al content in the 25 nm thick AlGaN layer was 25 %. The sheet resistance was 1260 Ω/sq., the sheet carrier concentration was approximately $5\times10^{12}\text{cm}^{-2}$, and the mobility was 1193 cm^2/V-s at room temperature, as determined by room temperature Hall measurements. Fabrication was performed in a similar manner to Section 2.2, with specific Ohmic contact resistance of 1.4x10^{-5} Ω-cm^2. PECVD SiN_x (100 nm) was deposited after the Ti/Al/Ni/Au Ohmic contacts. Contact windows were patterned in the SiN_x using a SF_6 RIE etch (details in Appendix III). Once we had etched the SiN_x down to the AlGaN layer, a Cl_2/BCl_3/Ar ICP etch was performed to form the recessed area. A 20 nm Ni/200 nm Au metal stack was then deposited to provide a gate contact. A schematic of the finished structure is shown in Fig. 2.26.

The gate recess ICP etch time was varied from 30 to 90 seconds in 15-sec. intervals. A control sample with no recess etching was provided for comparison. In addition, each etched sample had control HEMTs on the reticle which were not

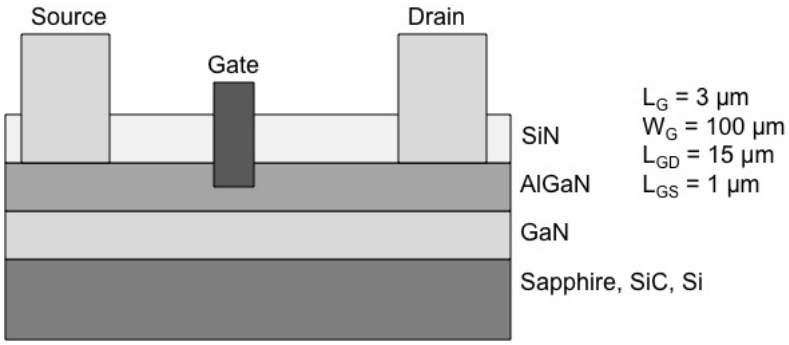

Figure 2.26: Cross section schematic of a recessed gate HEMT.

exposed to the dry etch, thus providing a direct comparison between etched and unetched (i.e., recessed and non-recessed) devices. Figures 2.27, 2.28, and 2.29 present the mobility, sheet resistance, and sheet carrier density as a function of etch depth. The mobility decreased over an order of magnitude, from 1100 to 100 cm^2/V-s, and sheet carrier density decreased from 5 to 1x10^{12} cm^{-2}, while sheet resistance increased orders of magnitude. Figure 2.30 shows the reduction of on-state current resulting from the decreased sheet carrier density.

The etch depth was measured using AFM microscopy on control samples with no gate metals and passivation SiN_x layer. Sample AFM images are shown in Fig. 2.31. The etch rate was almost linear (Fig. 2.32) with a rate of about 3 A/sec. At 90 seconds, the entire AlGaN layer was etched away. Note that for the longest etch time, the measured parameters became unrealistic, which was due to the very high resistance due to the absence of a conductive charge sheet.

The threshold voltage was extracted from the $\sqrt{I_{DS}}$-V_{GS} curves using the x-axis intercept of the curves. V_T approached 0 V as the AlGaN layer became thinner

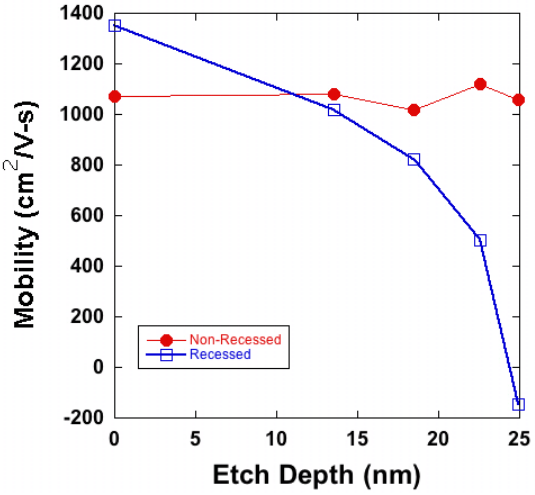

Figure 2.27: Mobility as a function of etch depth.

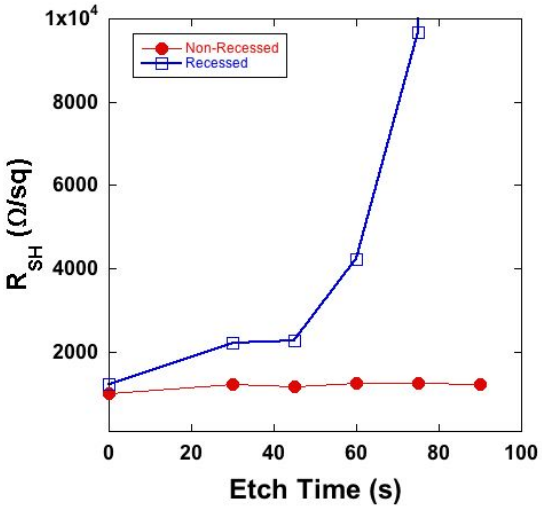

Figure 2.28: Sheet resistance as a function of etch depth.

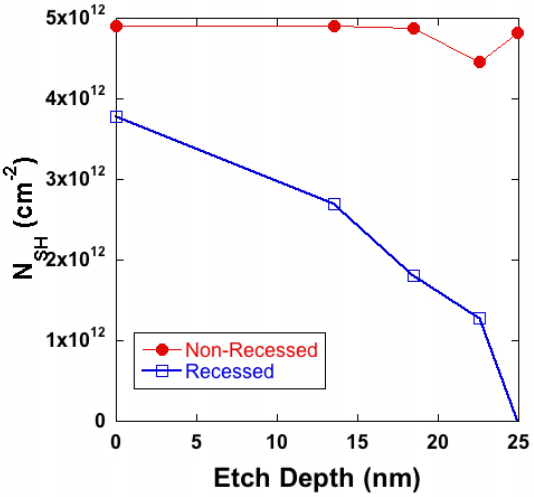

Figure 2.29: Sheet carrier density as a function of etch depth.

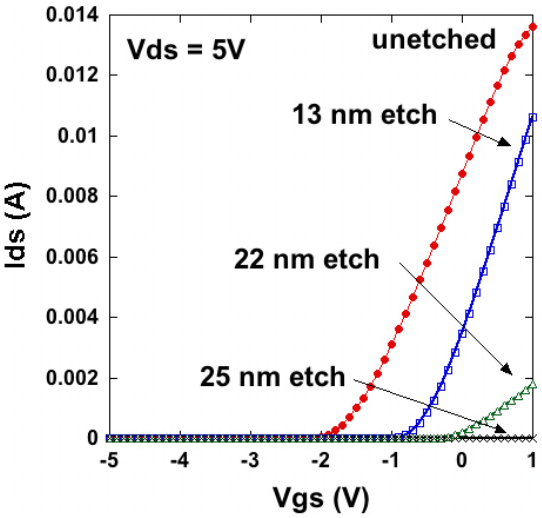

Figure 2.30: I_{DS}-V_{GS} curve showing threshold voltage shift as a function of etch depth.

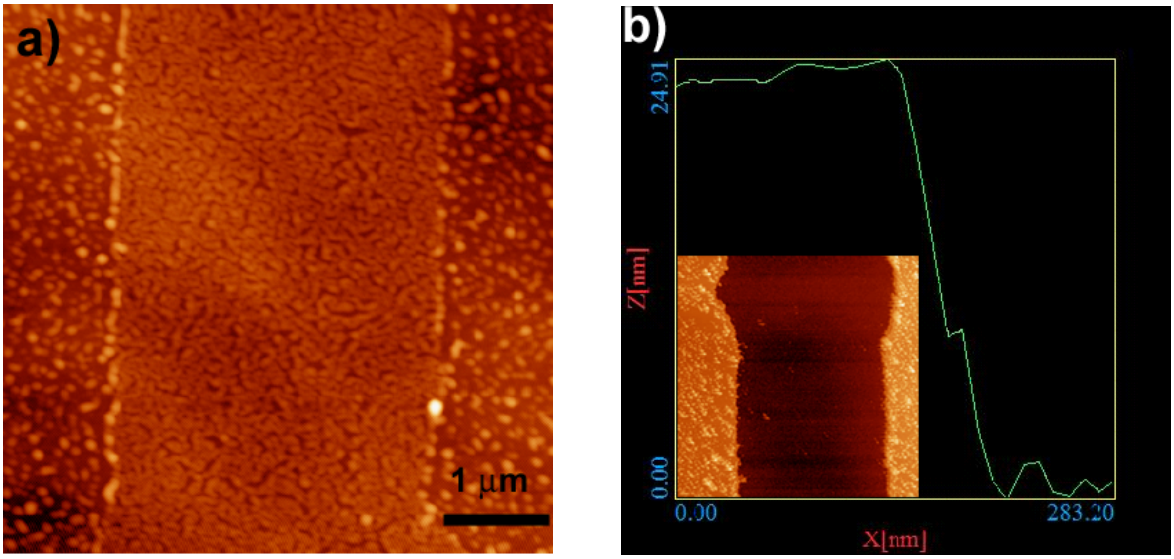

Figure 2.31: Atomic force microscopy images of the gate recess areas a) before and b) after 90 seconds of etching.

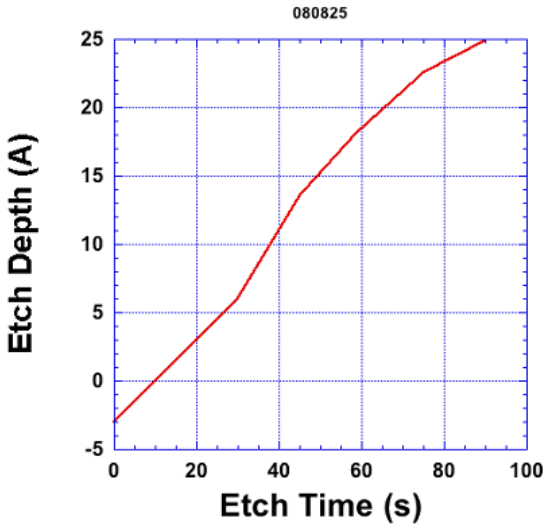

Figure 2.32: Measured recess etch depth as a function of ICP etch time.

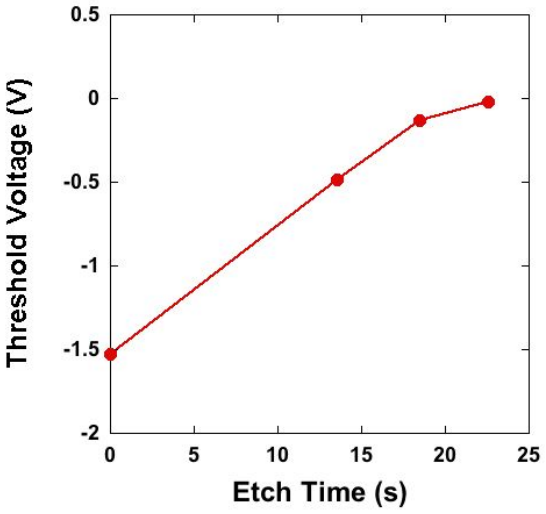

Figure 2.33: Extracted threshold voltage as a function of recess etch depth.

(increased recess depth), but the decreasing mobility and sheet carrier density only permitted functional devices at etch times up to 60 seconds. At that time, the thickness of the remaining AlGaN became less than the critical thickness required to form a 2DEG conduction channel. As a result, the drain current of the devices dropped several orders of magnitude down to the device isolation current (about 10 nA). However, the result is still consistent with the linear relationship given in Fig. 2.25.

It is interesting to note that even though V_T depends linearly with AlGaN thickness, the sheet carrier density does not. This difference is plotted in Fig. 2.34 and 2.35 for various Al concentrations.

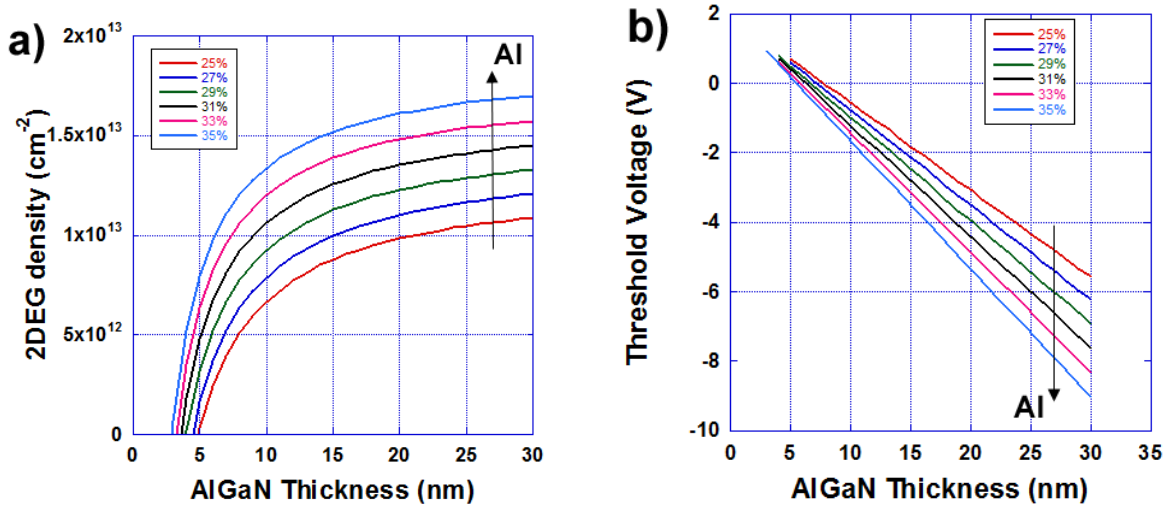

Figure 2.34: Dependence of HEMT a) sheet carrier density and b) threshold voltage on the AlGaN layer thickness, as a function of Al concentration [14].

The sheet carrier density was calculated using the following relation [14]:

$$N_{2D,R} = N_{2D}(1 - \frac{t_{CR}}{d}) \tag{2.2}$$

where $N_{2D,R}$ is the sheet carrier density in a recessed HEMT, N_{2D} is the sheet carrier density in a non-recessed HEMT, t_{CR} is the critical thickness of the AlGaN layer, and d is the AlGaN layer thickness after recess etching. The resulting threshold voltage decreases linearly with AlGaN layer thickness, as shown by eq. 2.3. The linear dependence is approximated by using qN_{2D} instead of $qN_{2D,R}$. Our ability to do so depends on the recess width. The narrower the gate, the more this approximation will hold.

$$V_T = \phi_B + \frac{qN_{2D}}{\varepsilon}(t_{CR} - d) \tag{2.3}$$

In the above expression, ϕ_B is the barrier height of the gate-AlGaN interface and ε is the dielectric constant of AlGaN. The critical thickness t_{CR} is given by

$$t_{CR} = \frac{(E_D - \Delta E_C)\varepsilon}{qN_{2D}} \tag{2.4}$$

where E_D is the surface level of the AlGaN layer (assumed as 1.65 eV) and ΔE_C is the conduction band offset in the heterojunction. As N_{2D} depends on the Al concentration as well, one could plot the critical thickness of AlGaN as a function of Al concentration.

This plot is intuitive because as the concentration approaches 0, the strain in the structure decreases as the lattice mismatch is eliminated and the thickness can be very high.

Electroluminescence characterization of the recessed-gate HEMTs revealed significant damage in the gate area. This contributed to the decreased mobility and

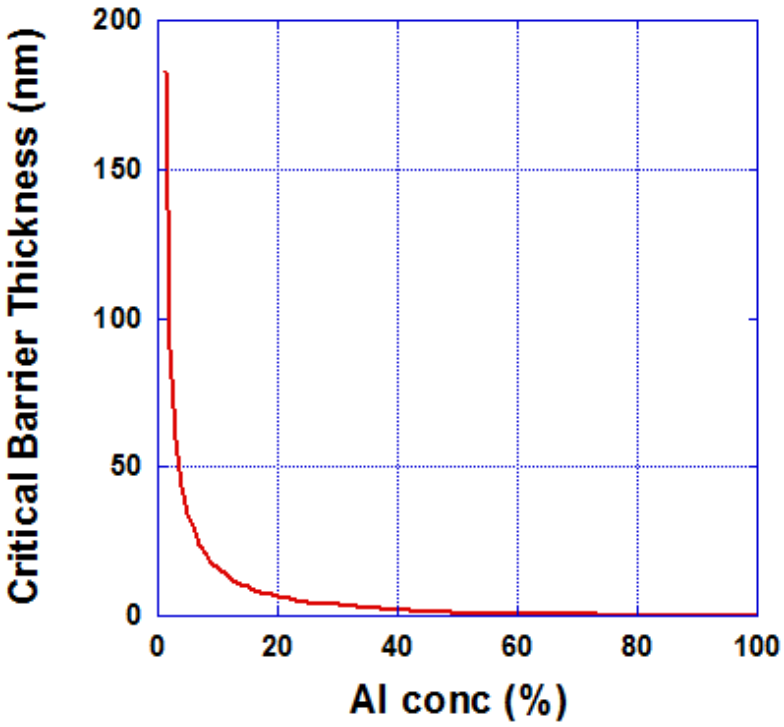

Figure 2.35: AlGaN critical thickness as a function of Al concentration.

increased sheet resistance. While many groups have devoted a significant amount of time to remedy the etch damage, mostly by means of annealing after the ICP etch, here we circumvent the problem by researching a wet etch process for the gate recess area. This approach is presented next.

2.3.2 AlN/AlGaN/GaN HEMT structure using a selective wet etch

While dry etching has been the most widely used method for demonstrate enhancement mode operation in AlGaN/GaN HEMTs, it has become clear that alternative methods need to be developed due to the lack of precise control in AlGaN etching. Stability of threshold voltage in a production environment can only be achieved if a highly controllable method of sheet charge reduction under the gate is found. Most recently, ion implantation of Fluorine ions had yielded stable V_T [93–95]. Still, exposure to Fluorine plasma necessitated a post-implant anneal.

On the other hand, wet etching of AlN has been known since 1995 [96]. This allowed us to pursue an AlN-based HEMT device, where a thin AlGaN layer serves both as an etch stop and as a sheet charge inducing layer away from the gate. However, the polarization charge provided by the thin AlGaN alone is not sufficient to support sufficiently high sheet charge in the source-drain access regions, thus an AlN cap is required to increase the polarization charge and reduce resistance.

The HEMT structure used in this study consisted of 4 nm AlN / thin $Al_{0.3}Ga_{0.7}N$ / 2 μm GaN layers grown on a-plane sapphire substrates by MOCVD. Two samples were grown: with 4 and 8 nm thick AlGaN layers, respectively. The 4 nm thick AlN cap was grown at 1050 ℃. The sheet resistance for both samples was approximately 1100 Ω/sq., the sheet carrier concentration was $6x10^{12}cm^{-2}$, and the mobility was about 1000 cm^2/V-s, determined at room temperature by Hall measurements. The formation of mesa and Ohmic regions was done using identical processing conditions to those in the previous Section. The measured specific contact resistivity was

$2x10^{-6}$ Ω-cm^2. Passivation using PECVD-deposited SiN_x (100 nm) was performed again, but this time this layer also served as an etch mask for the AlN layer.

The gate opening process was continued with selective chemical etching of the AlN using AZ400K developer at 85 ℃. It has been demonstrated that AZ400K developer selectively etches AlN over GaN [3, 15]. This approach is particularly unique as it allows for precise, repeatable control of threshold voltage with no etch-induced damage. Etch selectivity was verified using SEM imaging and electrical measurements of ungated HEMT devices, similar to those presented in Section 2.3.1. However, the etch time scale was a lot slower. While the gate recess area was etched at most 90 seconds using a dry etch, here we etched in 10 minute intervals, up to 70 minutes. Furthermore, SEM imaging showed the isotropic nature of the wet etch.

Finally, a Ni/Au gate was deposited using e-beam evaporation and patterned using a lift-off process. A schematic is shown in Fig. 2.36.

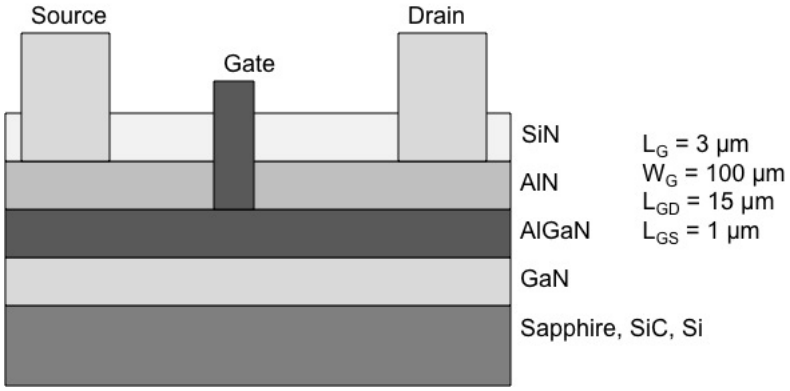

Figure 2.36: Cross section diagram of AlN/ultrathin AlGaN/GaN HEMT

A decrease in drain current similar to an ICP-etched HEMT was observed here as well, as shown in Fig. 2.37. After about 10 minutes of etching in AZ400K, the

device settled on a threshold voltage of about -0.5 V (Fig. 2.38), which value was consistent with theory. The linear dependence of V_T on the etch time observed in Fig. 2.33 was not observed here, even though the current continued to decrease as we etched for longer than 10 minutes. The reason for this is because once the AlN was etched down to the thin AlGaN layer, it continued to etch laterally instead of vertically, reducing the sheet carrier density away from the recess to the low value achieved in the recess area.

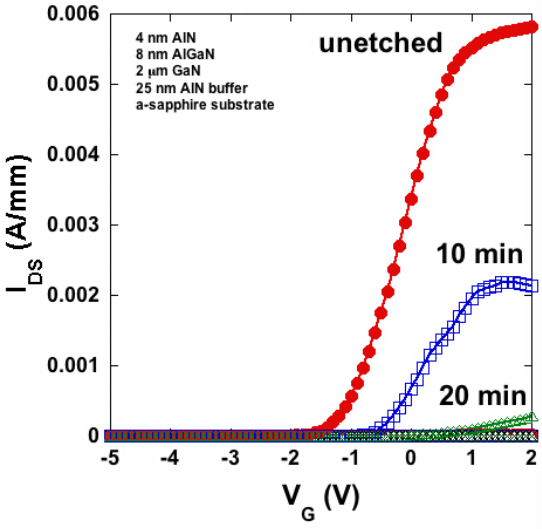

Figure 2.37: I_{DS}-V_{GS} curve at $V_{DS} = 5$ V showing threshold voltage shift with etching, but remaining constant once the AlN layer was etched away.

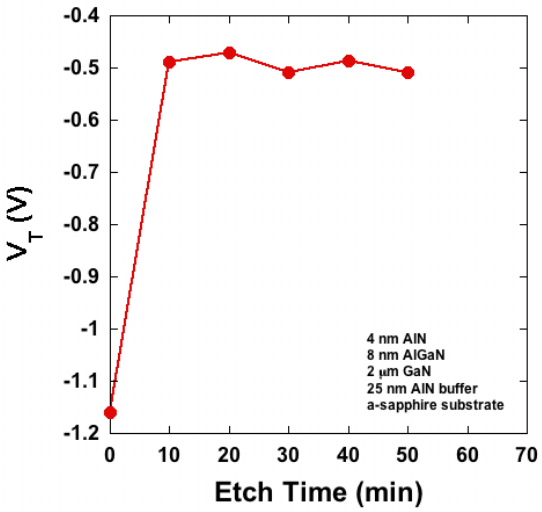

Figure 2.38: Threshold voltage as a function of etch time for the HEMT sample with 8 nm thick AlGaN layer.

Identical threshold voltage measurements were performed on the HEMT sample with a 4 nm thick AlGaN layer, and a value of +0.21 V was obtained from the $\sqrt{I_{DS}}$-V_{GS} plot for this sample (Fig. 2.39).

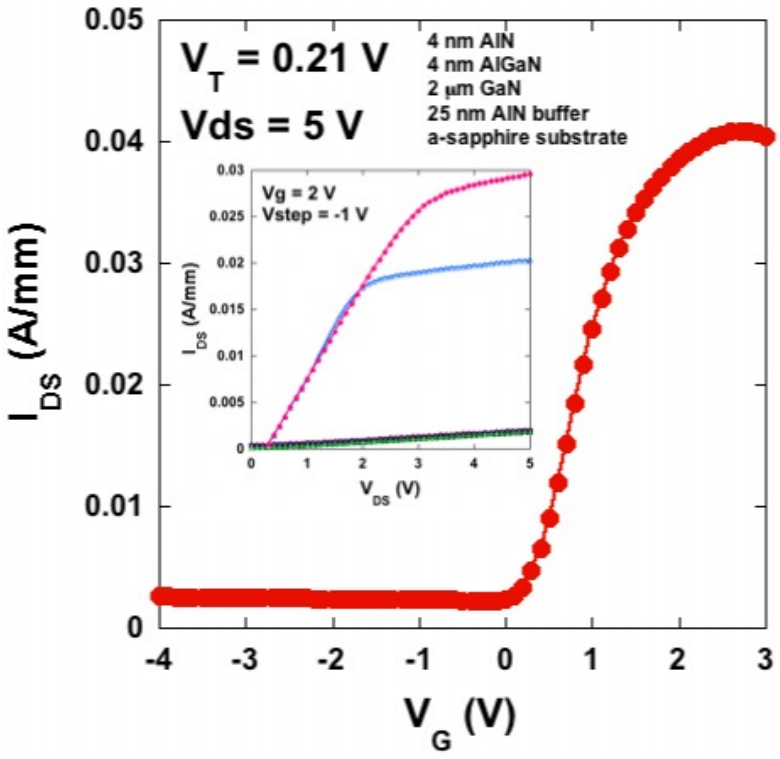

Figure 2.39: I_{DS}-V_{GS} curve for 4 nm AlN/4 nm AlGaN/2 μm GaN showing enhancement mode operation. I_{DS}-V_{DS} curve is shown as inset.

This value was reliably reproduced across the sample, which indicated that the wet etch process was more reliable and repeatable by avoiding any plasma damage. Hall effect measurements using van der Pauw structures after etching showed that mobility stayed high (710 cm^2/V-s).

2.4 Fabrication of GaN and AlGaN Accumulation-mode FET Devices

In developing III-Nitride based power switching devices, one could hardly imagine that FET devices could not offer potential benefits. Self-aligned processing and insulated gates have long been sought for the low device parasitic currents and capacitances they offer. The work presented here combines the wider band gap offered by AlGaN with a triple source/drain implantation scheme to compare accumulation-mode FET transistors (AccuFET) fabricated on GaN and AlGaN epitaxial layers.

Device fabrication was performed on two samples: a 2.5 μm GaN layer and a 2 μm $Al_{0.2}Ga_{0.8}N$ layer grown by MOCVD on sapphire substrates with a 500 nm thick AlN buffer layer. Both epitaxial layers were not intentionally doped. Subsequently, 100 nm thick SiO_2, followed by 500 nm of polysilicon, were deposited using LPCVD [97]. The polysilicon gate layer was degenerately doped by $POCl_3$ implantation, and patterned using an O_2-plasma RIE. Following that step, self-aligned source and drain ion implantation was performed using a box profile triple implant [98]. The dose and energy conditions for each implant were 1) $5x10^{15}$ cm^{-2} at 140 keV, 2) $5x10^{15}$ cm^{-2} at 100 keV, and 3) $2x10^{15}$ cm^{-2} at 40 keV. SRIM simulations calculated a 150 nm GaN implant depth profile for the 140 keV condition.

The polysilicon gate and GaN source/drain implants were annealed at 1050 ℃ for 5 min. in an N_2-purged furnace with ramp rate of about 80 ℃/min. The SiO_2 layer

was patterned using a CHF_3/O_2 RIE process (7 mT, 105 W, 1 sccm O_2 / 4 sccm CHF_3, etch rate of about 7 nm/min). Ohmic contacts were deposited by e-beam evaporation using Ti/Al/Ni/Au metals, and rapid-thermal annealed at 900 ℃ for 30 seconds in N_2 atmosphere. Sheet resistance R_{SH} and specific contact resistivity ρ_C for the implanted GaN and AlGaN regions were measured using the transfer length method (TLM). Instead of a mesa etch, a grounded Ohmic metal ring was present around the TLM contacts. The transistors fabricated using this process had annular geometry, with gate length variation from 1.8 to 7 μm and gate-source/drain spacing variation of 4, 5, or 6 μm. Fig. 2.40 shows a schematic representation of the fabricated devices.

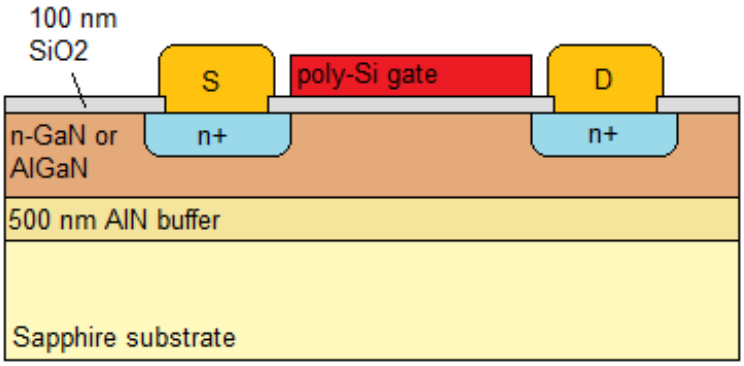

Figure 2.40: Schematic representation of GaN or AlGaN based accumulation-mode FET devices.

Presented on Fig. 2.41 are the resulting I_{DS}-V_{DS} characteristics for the GaN and $Al_{0.2}Ga_{0.8}N$ FET devices. All current-voltage measurements were performed using an HP4145B semiconductor parameter analyzer. Measured on-resistance for the GaN device with gate length of 5 μm was 43 kΩ at V_{GS} = 1 V, whereas the

AlGaN device with the same gate length yielded R_{ON} = 1.4 MΩ under the same bias conditions.

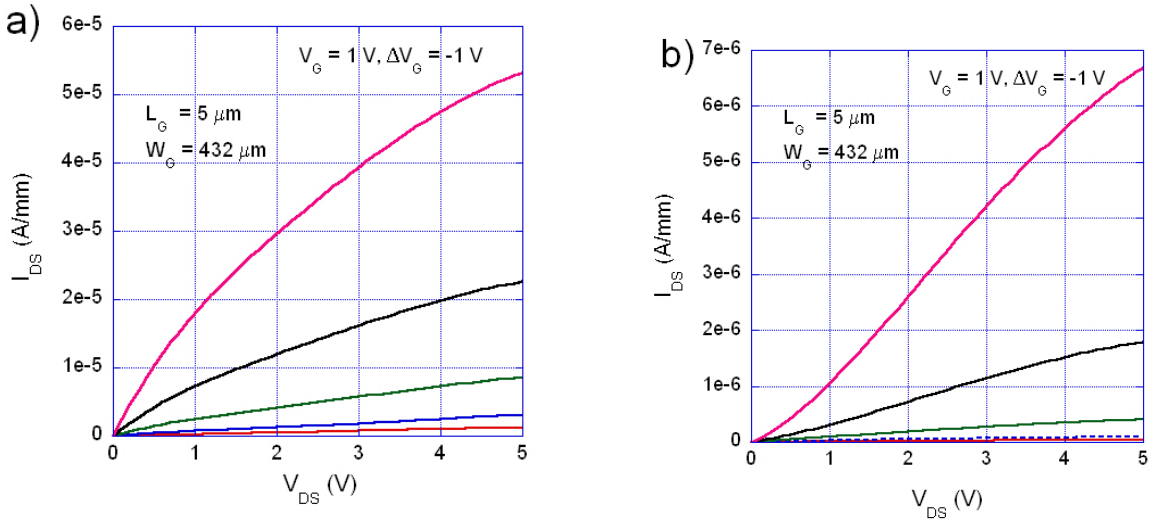

Figure 2.41: I_{DS}-V_{DS} characteristics for 2 um thick a) GaN and b) $Al_{0.2}Ga_{0.8}N$ accumulation-mode FET.

Figure 2.42 illustrates the dependence of the saturation drain current I_{DSS} on the gate length L_G and the source resistance.

Room-temperature measured parameters are summarized in Table 2.7. The large on-resistance was due to desorption of N atoms during the source/drain implant anneal. The resulting Ga-rich surface, in addition to the activation of implanted Si ions, resulted in the low sheet resistance of the implanted regions ($R_{SH,n+}$). The on-resistance can be significantly reduced by incorporating an AlN capping layer during annealing. In addition, a post-implant gate oxide deposition step using a non self-aligned process would allow for higher annealing temperature of the Si implant, resulting in even higher current density.

Temperature-dependent measurements of drain current are presented on Fig. 2.43.

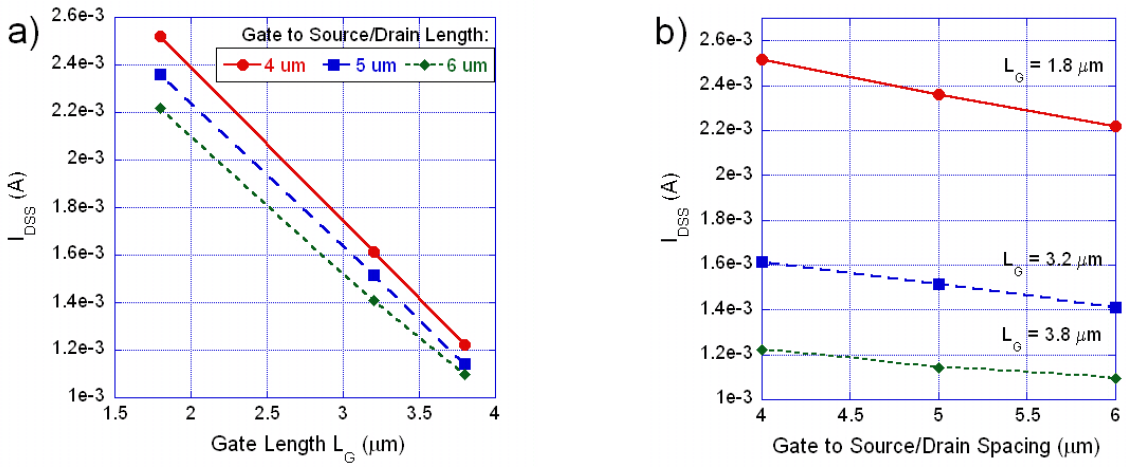

Figure 2.42: Saturation current I_{DSS} at V_{GS} = 1 V and V_{DS} = 5 V for the GaN FET as a function of a) gate length L_G and b) gate to source/drain length.

Table 2.7: Summary of GaN and $Al_{0.2}Ga_{0.8}N$ AccuFET parameters.

	GaN FET	$Al_{0.2}Ga_{0.8}N$ FET
$R_{SH,n+}$ (Ω/sq.)	115.9	111
$\rho_{C,n+}$(Ω-mm)	0.137	0.359
$\rho_{C,n+}$(Ω-cm^2)	1.61x10^{-6}	1.16x10^{-5}
$V_{TH,30°C}$ (V)	-6	-4.65
R_{ON} (Ω)	43k	1.4M

The maximum drain current I_{DSS} increased by almost an order of magnitude when measured between 30 to 210 ℃, despite the increase of threshold voltage within the same temperature range (Fig. 2.44b). Therefore, the accumulation channel density increased as the polarization charge on the GaN epilayer back side became more positive at higher temperatures [99]. The extremely thick AlN buffer layer (500 nm)

resulted in a relaxed device layer, with polarization charge density dominated by the spontaneous component, rather than the piezoelectric component.

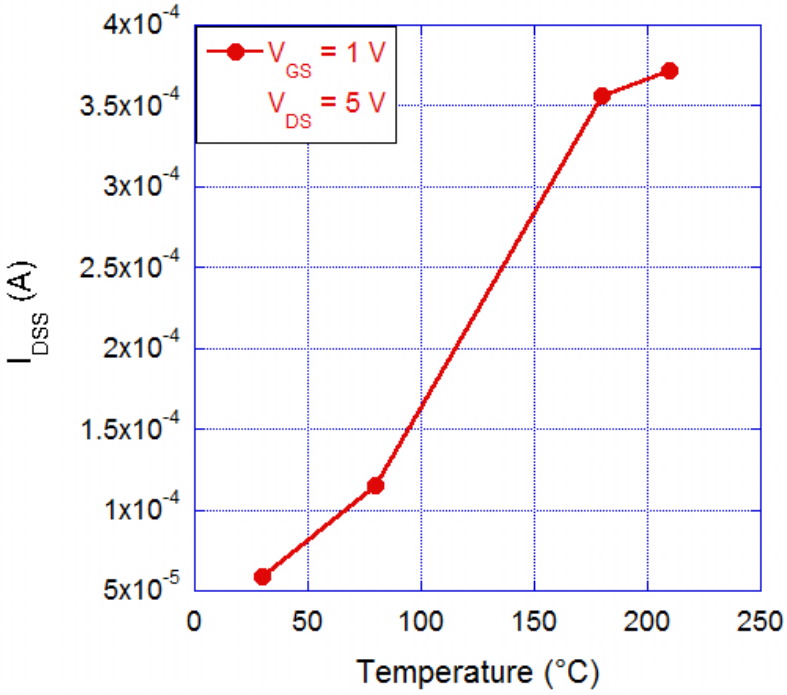

Figure 2.43: Saturation current I_{DSS} at V_{GS} = 1 V for the GaN FET as a function of temperature.

Threshold voltage control has been a central problem in the fabrication of III-Nitride MOS devices. Matocha et. al. were able to shift V_T towards positive values by creating a back side depletion region using an AlGaN buffer layer [97]. In this work, backside leakage reduction using a 2 μm AlGaN epilayer resulted in a threshold voltage shift from –6 V for the GaN to –4.65 V for the AlGaN device. The values of V_{TH} were extracted from the x-axis intercept of the linear fit of the I_{DS}-V_{GS} curves on Fig. 2.44a.

The extremely low gate leakage allowed the electron concentration of the epi-

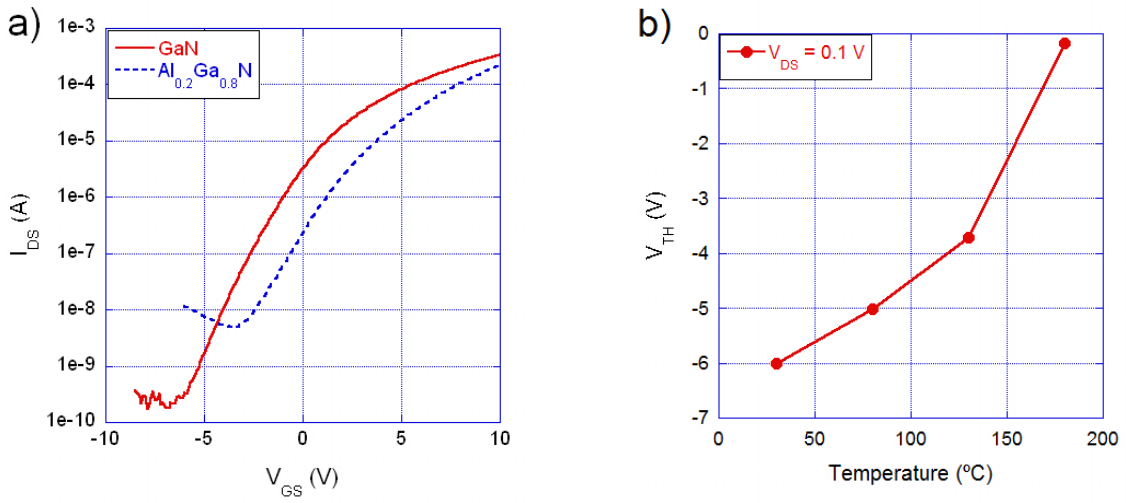

Figure 2.44: a) I_{DS}-V_{GS} plot for GaN and $Al_{0.2}Ga_{0.8}N$ FETs (V_{DS} = 1 V). b) Threshold voltage as a function of temperature for GaN FET extracted at V_{DS} = 0.1 V.

taxial GaN to be extracted using capacitance-voltage measurements, performed at 100 kHz using a Keithley 590 LCR meter. Analysis of the C-V curve yielded a carrier concentration of 7x10^{15} cm^{-3}. Higher gate leakage ($I_G \cong$ 1 μA) prevented capacitance-voltage analysis on the AlGaN-based FET. The AlGaN FET also had higher off-state drain current leakage than the GaN-based FET (Fig. 2.44a), possibly resulting from reduced channel pinch-off due to higher non-intentional doping in the device layer.

2.5 Chapter Summary

In this chapter, we have demonstrated a basic process for the fabrication of AlGaN/GaN high electron mobility transistors. In addition, two approaches for the fabrication of enhancement mode HEMT devices were explored. Both relied

on a recess etch under the gate, using either a dry or a wet etch. As expected, the thinning of the AlGaN layer decreased the mobility and the sheet resistance of the device. Even though a number of papers have predicted or measured this phenomenon, it has never been systematically studied. For both approaches, the threshold voltage approached zero, accompanied by a rapid drop in I_{DS}. Threshold voltage of +0.2 V is reported for the wet-etched AlN/AlGaN/GaN HEMT.

Accumulation-mode GaN and AlGaN field-effect transistors were fabricated on sapphire substrates using an LPCVD-deposited SiO_2 gate oxide and triple-implanted source/drain regions. The saturation-mode drain current (I_{DSS}) increased with temperature due to more positive polarization charge on the back side Ga-face of the epilayer. However, hot electron effects countered that increase at high drain biases above 100 ℃. Room-temperature threshold voltage measurements indicated a higher V_{TH} for the AlGaN device. For the GaN device, threshold voltage increased from -6 V to -0.2 V when measured between 30 to 210 ℃.

Chapter 3

Reduction of Self-Heating Effects in AlGaN/GaN HEMTs by Incorporation of Nanocrystalline Diamond Heat Spreading Films

Recent major advances of diamond growth using chemical vapor deposition (CVD) have spurred intense research within the semiconductor industry in order to take advantage of its high thermal conductivity κ (above 1800 W/m-K). While development of diamond integration technology could enable a revolution in integrated circuit cooling, current CVD diamond growth has the potential to provide cooling for discrete power devices. As the requirements for higher device power and switching frequency in next-generation converters increase, more efficient cooling schemes will be necessary.

High electron mobility transistors (HEMTs) based on the AlGaN/GaN heterostructure are excellent candidates for commercial high temperature power switching applications due to the wide band gap of the III-N material system. The reduction of drain current at high drain bias, referred to as self-heating, is a phenomenon well-documented in the literature [76, 82–84, 100, 101]. Despite the attractive properties of CVD diamond, device thermal budget requirements have limited the diamond growth temperature in the past [85]. In this work, we present an AlGaN/GaN HEMT with integrated nanocrystalline diamond (NCD) thin films. The NCD films were grown at 750 ℃ prior to HEMT gate formation. This approach has allowed us

to provide a heat spreading channel immediately adjacent to the heat source in the device, i.e., the channel area underneath the gate.

3.1 Characterization of NCD-Capped AlGaN/GaN HEMT Structures

Epitaxial layers of 20 nm AlGaN and 2 μm GaN were grown on high-resistivity n-type Si substrate via MOCVD. The AlGaN and GaN epilayers were lightly doped n-type with Si. A 50 nm SiN_x layer was deposited via Plasma Enhanced CVD (PECVD) on all samples except one (sample 6, Table 3.1). The presence of SiN_x helped the nucleation of NCD on the underlying AlGaN/GaN structure. To study the conduction mechanism between NCD and GaN, a sample without the AlGaN layer was prepared as well. A 0.5 μm thick NCD film was grown on a 1.0 μm thick unintentionally n-doped ($N_D \cong$ 1-5x10^{15} cm^{-3}) GaN epilayer on an n^+ doped (111) Si substrate. In general, sapphire substrates were avoided due to the large thermal mismatch between NCD and sapphire, which caused NCD films to exfoliate during post-deposition cooldown. Details of the NCD growth can be found in section 5.1.

Using e-beam evaporation, 300 nm thick Al contacts were deposited. No post-evaporation annealing was performed. For device isolation, NCD mesas were etched in an O_2-RIE system using the Al layer as a mask. In addition to the diode structures, TLM structures were fabricated for sheet resistance and specific contact resistivity measurements. Figure 3.2 presents the results of linear TLM measurements for sample 2, which had a SiN_x nucleation layer deposited on the AlGaN prior to

NCD growth [102]. Table 3.1 summarizes the results for all six samples.

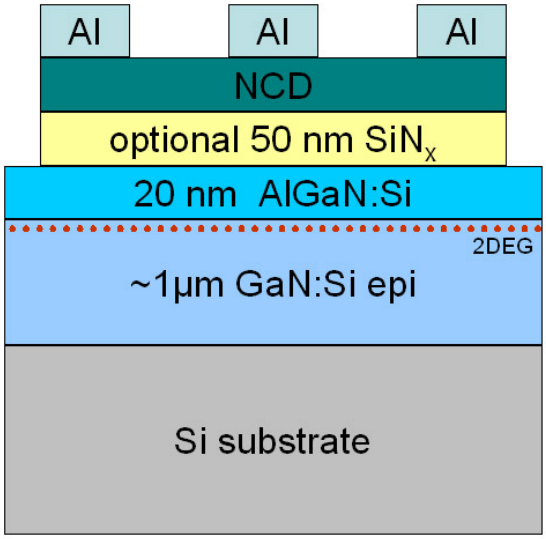

Figure 3.1: Sample structures in this work

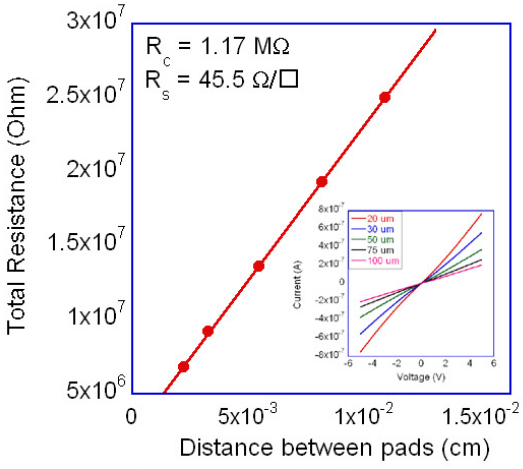

Figure 3.2: Transfer length method (TLM) characteristics of sample #2 (see Table 3.1).

The sheet resistance of the AlGaN/GaN 2D electron channel was measured before and after NCD deposition using a Lehighton LEI-1510 mapper. The results are summarized in Table 3.1. For samples 1 through 5, a decrease in sheet resistance was observed after SiN_x and NCD deposition. This ΔR_{SH} could possibly be due to fixed charge incorporated in the NCD layer or strain induced by the either the NCD or the SiN_x layer.

To determine whether the NCD or the SiN_x layer had caused the change in sheet resistance, a new sample was fabricated, with the same structure as sample 1. The mobility, sheet resistance, and Raman spectra were measured before and after SiN_x deposition, as well as after NCD deposition. The mobility measurements were

Table 3.1: AlGaN/GaN 2D electron channel sheet resistance, contact resistance, and Raman peak shift measurements before and after NCD deposition on samples with (samples 1-5) and without (sample 6) a SiN_x nucleation layer.

Sample #	SiN_x present?	d_{NCD} (um)	t_{SEED} (min)	Rs_1 $\Omega/sq.$	Rs_2 $\Omega/sq.$	ΔRs $\Omega/sq.$	ρ_c $\Omega-cm^2$	Rs_{NCD} $\Omega/sq.$	$\Delta - peak$ (cm^{-1})
1	Yes	0.21	15	300	285	15	512	6.69x10^8	
2	Yes	0.21	10	275	250	25	468	4.55x10^7	
3	Yes	0.10	5	275 287 300	241 257 289	34 30 11	127.2 110.4 128.8	2.68x10^7 2.20x10^7 2.34x10^7	0.78 1.21 0.63
4	Yes	0.35	1	300	289	11	35.28	1.08x10^7	0.8
5	Yes	0.35	10	287 300	268 291	21 9	323.6 200	4.14x10^7 3.93x10^7	
6	No	0.5	20	N/A	5500	N/A	2.82x10^4	2.10x10^8	

Legend:
d_{NCD} – thickness of NCD films
t_{SEED} – seeding time before NCD growth
Rs_1 – initial sheet resistance of the AlGaN/GaN HEMT
Rs_2 – sheet resistance measured after SiN_x deposition and NCD growth
$\Delta Rs = Rs_2 - Rs_1$ – difference in sheet resistances
ρ_C – specific contact resistivity
Rs_{NCD} – sheet resistance of the NCD film measured by TLM
Δ-peak – Shift in Raman TO phonon peaks after SiN_x deposition and NCD growth

performed using a Lehighton 1610 non-contact mobility measurement system [103].

The most important result from Table 3.2 is the observation that the 2D electron channel mobility did not degrade as a result of the NCD deposition at 750 ℃. This encouraging result enables further research into the application of NCD as a topside heat sink for HEMT devices.

The influence of the NCD and SiN_x layers on the strain in the AlGaN layer was studied using Raman spectroscopy [104]. Raman scattering was excited via a 532 nm

Table 3.2: Separation of the effect of SiN_x and NCD deposition on AlGaN/GaN 2D electron sheet resistance and channel mobility.

Sample #	Rs_1 (Ω/sq.)	Rs_2 (Ω/sq.)	Rs_3 (Ω/sq.)	μ_{HALL1} (cm^2/Vs)	μ_{LEH2} (cm^2/Vs)	μ_{LEH3} (cm^2/Vs)
7	679.0	680.0	574.5	861.42	1135	1016.25

Legend:
Rs_1-– initial sheet resistance on unprocessed AlGaN/GaN HEMT measured using Lehighton 1510
Rs_2 – sheet resistance measured after 50 nm PECVD SiN_x deposition
Rs_3 – sheet resistance measured after 0.5 μm NCD deposition
μ_{HALL1} – Hall mobility measured on the unprocessed AlGaN/GaN HEMT sample
μ_{LEH2} – mobility measured after 50 nm PECVD SiN_x deposition using Lehighton 1610.
μ_{LEH3} – mobility measured after 0.5 μm NCD deposition using Lehighton 1610.

diode laser directed through a Mitutoyo microscope and a 50x (0.7 NA) objective. The excited spectra were collected using an Ocean Optics QE65000 spectrometer through a 600 um optical fiber. As evident from Figure 3.3, the SiN_x layer attenuated the Raman signal from the underlying layers. However, its absence introduced a peak at 480 cm^{-1}, which could be due to the presence of Boron Carbide. The triple SiN_x structure around 250-400 cm^{-1} and the broad peak at 701 cm^{-1} were introduced upon deposition of the SiN_x and NCD layers.

In addition, Raman characterization was performed on sample 7 (Table 3.2), before and after SiN_x deposition, and after NCD deposition. Figure 3.4 shows the resulting GaN Raman shifts after each step. In two out of three cases, we found that the NCD layer had negligible effect on the shift in the GaN TO peak.

Current-voltage measurements were performed on sample 6 (no nitride) in order to study the conduction mechanism between NCD and the AlGaN/GaN structure. Using an HP4145B semiconductor parameter analyzer, the samples were mea-

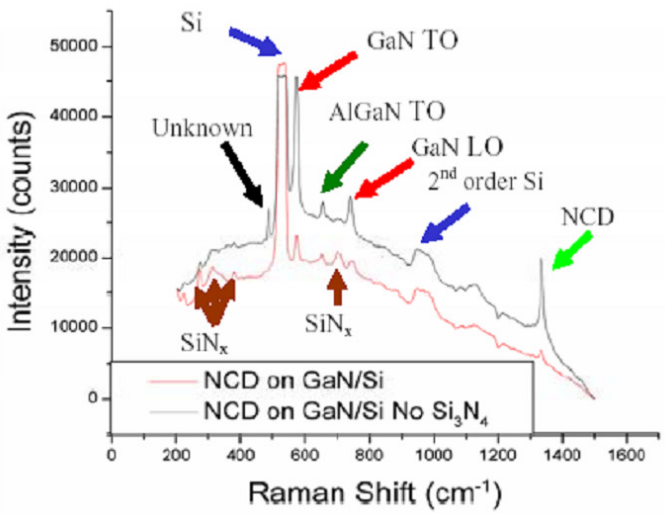

Figure 3.3: Raman spectra of NCD thin films grown on AlGaN/GaN with or without a SiN_x buffer layer.

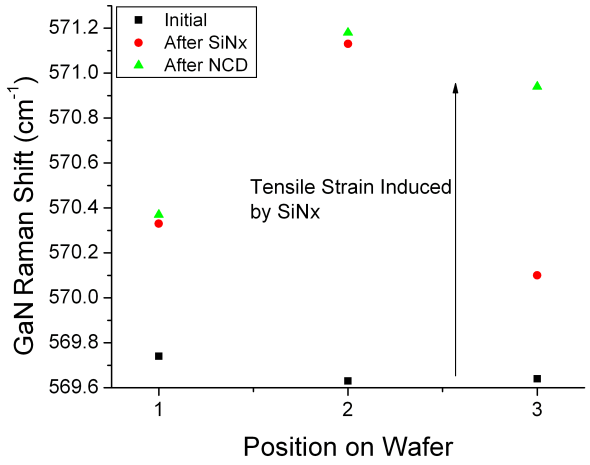

Figure 3.4: Raman spectra of NCD thin films grown on AlGaN/GaN with a SiN_x buffer layer.

sured either from one topside contact to another topside contact (front to front), or from a topside contact to the back side of the Si substrate (front to back), as shown

in Figure 3.5.

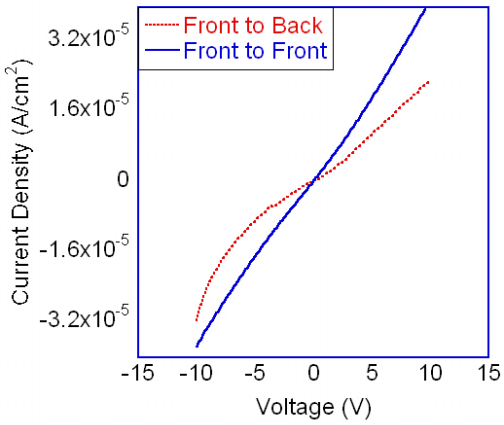

Figure 3.5: I-V characteristics of NCD grown on AlGaN/GaN without a SiN_x layer.

The non-rectifying conduction behavior in this Type-II heterojunction could be explained by trap-assisted tunneling between the AlGaN conduction band and the NCD valence band or boron acceptor levels. Ideally, the difference between the conduction band of GaN and the NCD valence band is only 0.2 eV [1, 105]. In this case, the Fermi level of the boron acceptors would be up to 0 - 0.1 eV below the GaN conduction band, and tunneling probability is high. The situation changes when AlGaN is introduced into the system. Due to the uncertainty of the values for the AlGaN electron affinity reported in the literature, a value linearly extrapolated between AlN and GaN was used. This value increased the difference between the AlGaN conduction band and the NCD valence band to more than 0.6 eV. Therefore, trap-assisted tunneling had to rely on deeper NCD levels as well. Further studies of deep levels in NCD films are presented in Chapter 5.

3.2 Development of NCD-Capped HEMT Devices

Following the encouraging results from the previous section, here we present the implementation of an AlGaN/GaN HEMT with NCD thin films incorporated for the purpose of local heat spreading. The HEMT structures were obtained from Nitronex Co. on Si substrates, which facilitated NCD process integration due to their better thermal conductivity and better thermal expansion coefficient match to NCD than sapphire substrates.

What is really needed is a high thermal conductivity material situated in close proximity to the thermal source in the device. This approach was attempted by Seelmann-Eggebert et al. in 2001 [85]. CVD diamond was deposited upon a fabricated device, which introduced a tradeoff between the Schottky gate quality and the deposition temperature. To maintain reasonable gate contact quality, NCD deposition temperature was limited to 500 ℃. However, NCD quality was also sacrificed by using this "diamond-after-gate" approach.

Our approach focused on depositing the NCD heat spreading films prior to HEMT gate fabrication (a.k.a. "diamond-before-gate" method). In this way, thermal damage to the device contacts was minimized and functional devices were obtained. The main processing challenges during device fabrication were to ensure device functionality after prolonged high-temperature diamond growth, develop a reliable diamond etching process, and provide adequate electrical channel isolation using an appropriate insulator without sacrificing the thermal benefits of the diamond film. Each of these requirements presented its own set of trade-offs, which

will be described in detail below.

A concept of a diamond-cooled HEMT structure is shown in Fig. 3.6. A detailed process sheet for fabricating this structure is given in Appendix III.

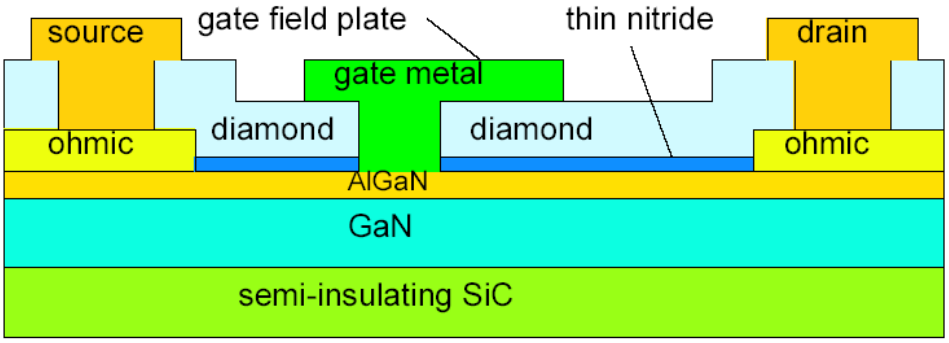

Figure 3.6: AlGaN/GaN HEMT fabricated using a "diamond-before-gate" fabrication process.

In the previous section, we had presented Hall measurements of AlGaN/GaN HEMT structures before and after NCD growth. The next step was to fabricate HEMT structures with NCD capping layers. However, it was necessary to also provide control samples to separate the effect of thermal stress due to NCD growth from the effects of the NCD itself. For this reason, we first fabricated HEMT devices and exposed them to thermal anneals in a furnace at similar conditions to those of NCD growth (750 ℃, 5 hours, N_2 flow). The devices had either no dielectric cap, a SiO_2 cap, an Al_2O_3 cap. The anneals were performed after Ohmic contact deposition, but before gate deposition, in a fabrication sequence identical to that of an NCD-capped HEMT but with a 5 hour anneal instead of a 5 hour NCD deposition step. The I_{DS}-V_{DS} of the three HEMTs after annealing are shown in Fig. 3.7.

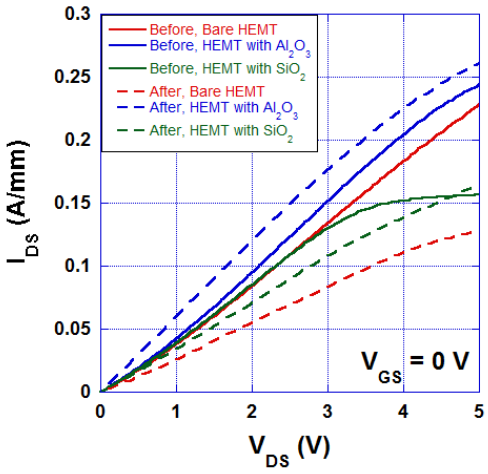

Figure 3.7: Open-gated (V_{GS} = 0 V) characteristics of HEMTs before and after annealing.

The largest degradation in current occurred on the sample with no dielectric cap. SEM images of the devices' surface were taken and are included in Appendix I. Clearly, the Al_2O_3 cap did not hold up to the high temperature, and that was reflected on the I_{DS}-V_{DS} measured after a gate was deposited (Fig. 3.8b). The sample with a SiO_2 cap exhibited the lowest current density (0.06 A/mm at V_{DS} = 10 V), but was otherwise functional (Fig. 3.8c). A sample with a SiN_x cap was annealed under the same conditions as well, and even though the material parameters shown in Section 3.1 were favorable for the HEMT to withstand high temperatures, the gated device did not modulate (Fig. 3.8d).

In addition to the annealing temperature and duration, the atmosphere to which the HEMT structure was exposed during diamond growth had to be also evaluated for its influence on the HEMT performance. Typically during the CVD

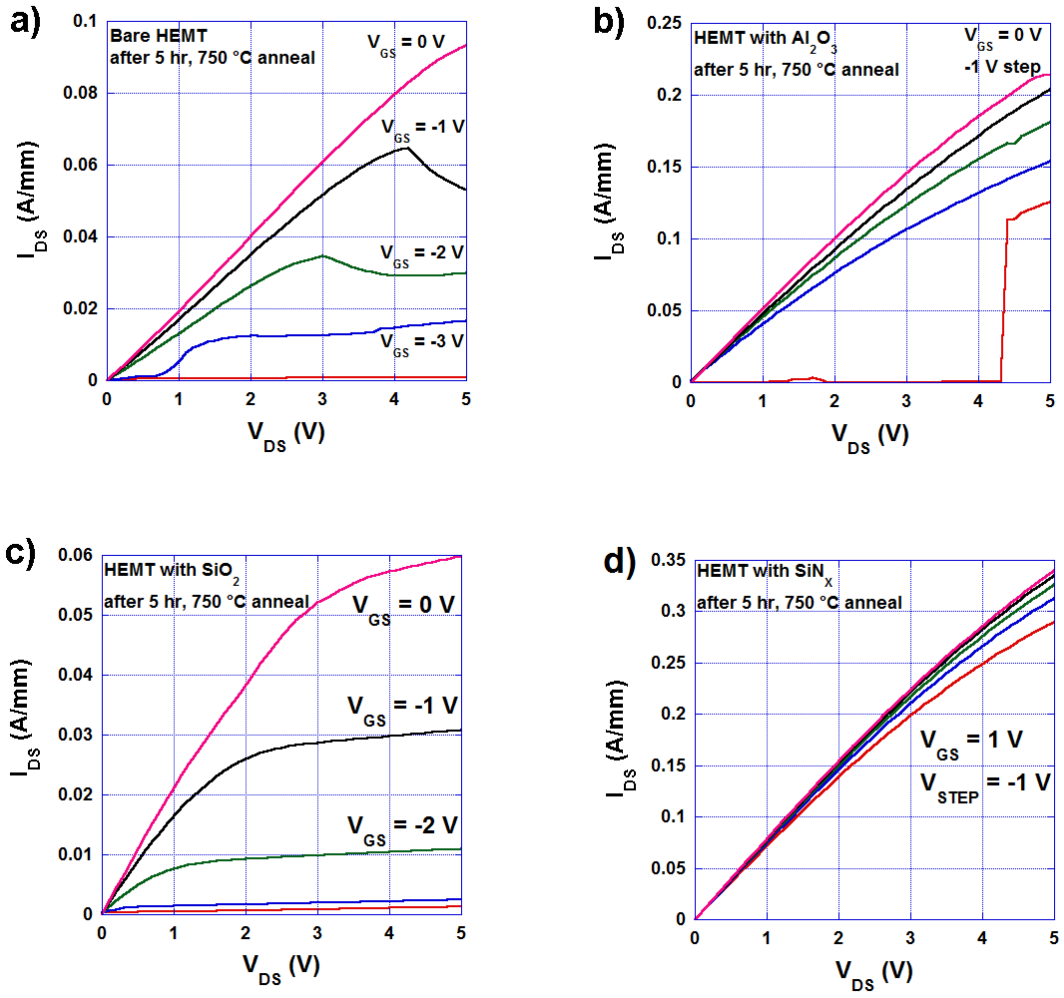

Figure 3.8: Current-voltage characteristics of annealed AlGaN/GaN HEMTs with a) no dielectric cap, b) Al_2O_3 cap, c) SiO_2 cap, and d) SiN_x cap.

process, the diamond films are grown in the presence of Hydrogen (details on CVD growth of diamond are given in Chapter 5). Therefore, we conducted anneals in forming gas (about 5 % H_2 in N_2) and pure N_2, and compared these samples to ones with CVD diamond. The results are given in Table 3.3, and it can be seen that the atmosphere of growth did not significantly influence the device parameters.

Table 3.3: HEMT thermal stress measurements.

	N_2 Anneal		N_2/H_2 Anneal		Diamond	
	Before	After	Before	After	Non-etched	Etched
R_{SH} (Ω/sq.)	429	417	443	409	418	411
μ_h (cm^2/V-s)	1590	1660	1560	1650	1650	1670
N_{SH} (cm^{-2})	$9.14x10^{12}$	$9.04x10^{12}$	$9.05x10^{12}$	$9.25x10^{12}$	$9.05x10^{12}$	$9.11x10^{12}$

Following this initial characterization, a set of HEMT transistors was fabricated and capped with NCD films. For HEMT fabrication, the NCD etching process was modified from an 200 W RIE to a 1000 W ICP-based recipe with a much faster etch rate to reduce plasma damage and improve NCD etched surface morphology. The details of the NCD etch optimization process, along with the relevant SEM images, are given in Appendix I.

Initially, the dielectric of choice for NCD nucleation was PECVD deposited SiN_x. Even though it was demonstrated in the previous section that the channel mobility and sheet resistance remained almost unchanged, HEMT fabrication resulted in non-modulating devices. On the other hand, the experiment from Table 3.3 showed that PECVD deposited SiO_2 could hold up better to thermal stress caused by NCD growth. With a SiO_2 diamond nucleation layer, the HEMT gate leakage was reduced by several orders of magnitude. In addition, the devices were able to take advantage of the approximately a factor of two higher thermal conductivity of SiO_2 (approx. 1 W-m^{-1}-K^{-1} for PECVD SiO_2 vs. 0.5 W-m^{-1}-K^{-1} PECVD SiN_x) to improve the heat spreading ability of the NCD capping layers [106]. Finally, the optimal thickness of the SiO_2 layer was determined to be 50 nm. Thinner SiO_2 resulted in excessive gate leakage current, whereas thicker SiO_2 increased the distance

between the NCD and the gate (heat source), rendering the heat spreading process less effective.

3.2.1 Simulation of Self-Heating Effects

The main purpose of such simulations was to determine the optimal NCD heat spreading layer dimensions. Figure 3.9 presents an ANSYS simulation of a 2 μm GaN on SiC structure with a T-gate, without and with a 2 μm diamond cap, respectively. The simulations were performed by Dr. Jeff Calame at the Naval Research Laboratory, and have been used here as an example of the effect of diamond on the HEMT temperature. On Figure 3.9, the maximum calculated temperature at the gate was 133 ℃, and was reduced to 78 ℃ once the diamond cap was added.

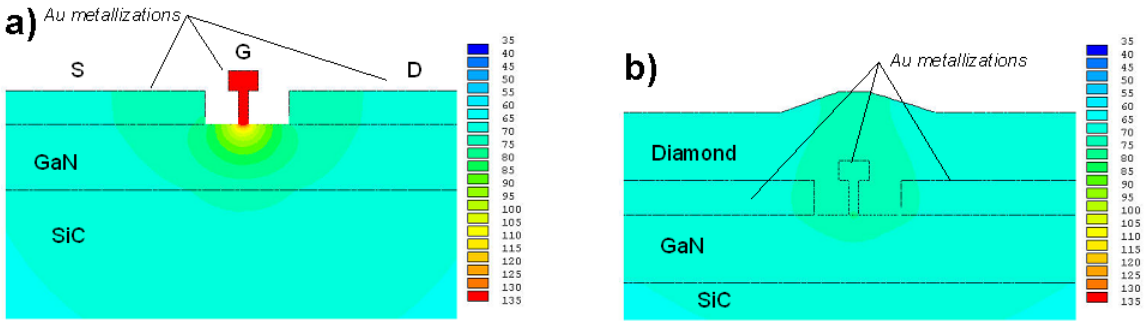

Figure 3.9: Simulation of a concept GaN device on a SiC substrate with Au contacts at 5 W/mm power dissipation a) without and b) with a diamond cap. The temperature scale is in ℃.

The above simulations agree well with the channel temperature measurements presented on Figure 2.17. In the actual implementation, the NCD layer did not exceed 0.5 μm thickness, due to its relatively low growth rate (0.1 μm/hr). A

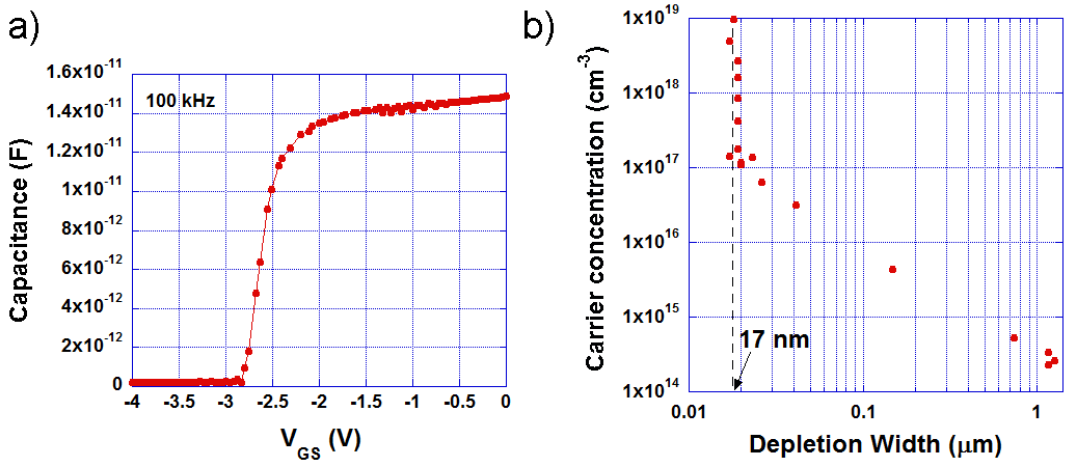

Figure 3.10: a) High frequency (100 kHz) capacitance-voltage curve of the Schottky gate of an AlGaN/GaN HEMT. b) Carrier concentration vs. depletion width extracted from the C-V curve.

thinner NCD layer implies less efficient heat spreading capability, which may be compensated with extending the lateral dimensions of the NCD layer. However, this would increase the source and drain resistances, since it pushes the source and drain contacts farther from the gate. This tradeoff would have to be carefully studied in the future.

3.2.2 NCD Integration in Insulated-Gate HEMT Devices

The HEMT devices used in this experiment were fabricated on 2 nm/17.5 nm/2 μm thick GaN/$Al_{0.26}Ga_{0.74}N$/GaN structures on float-zone (111) Si substrates. The AlGaN layer thickness was verified by capacitance-voltage measurement of the 2DEG carrier concentration, as shown in Fig. 3.10.

At gate voltage above threshold, the 2DEG was present and the measured

carrier concentration was very high at a depletion width that corresponded to the thickness of the undoped (depleted) AlGaN layer. As V_{GS} decreased below threshold, the depletion region extended into the GaN layer.

The material was grown by metal organic chemical vapor deposition by Nitronex, Inc. The sheet resistance was around 557 Ω/sq., measured using a Lehighton probe and confirmed by Hall measurements on subsequently fabricated test structures [102].

3.2.2.1 Fabrication Details of NCD-capped HEMTs

The HEMT devices were isolated on mesa regions, etched in a Cl_2/Ar inductively coupled plasma (ICP) system (10/5 sccm Cl_2/Ar, 5 mTorr, 150 W ICP, 40 W RF, 60 nm/min). Ohmic contacts were deposited by e-beam evaporation of 20/120/40/50 nm of Ti/Al/Ni/Au and rapid-annealed at 900 ℃ for 30 sec under flowing N_2. The specific contact resistivity ρ_C obtained was 1.71x10-6 Ω/cm2 (0.309 Ω-mm). A 50 nm thick layer of PECVD SiO_2 was deposited to serve both as a surface passivation layer [17] and a NCD nucleation layer. The 0.5 μm thick NCD layer was grown at 750 ℃ at a rate of about 100 nm per hour, unintentionally B-doped for p-type conductivity. Details of NCD seeding and growth are reported elsewhere in the literature [4, 107, 108]. The grain size of the NCD film was less than 300 nm, depending on the growth time. The NCD film was etched over the contact areas using an O_2-based ICP process (50 sccm O_2, 15 mT, 1000 W ICP, 100 W RIE, about 180 nm/min etch rate) using a 100 nm thick PECVD SiN_x etch

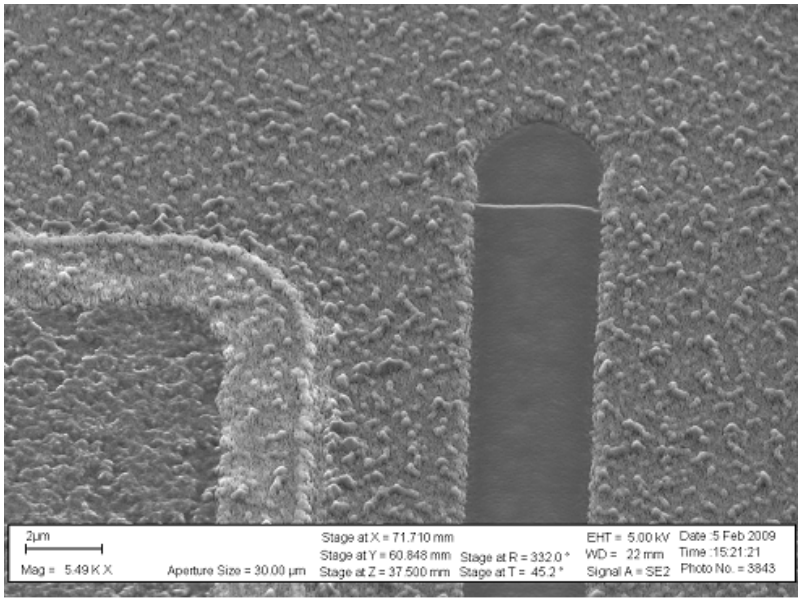

Figure 3.11: Scanning electron micrograph of the channel area of the fabricated AlGaN/GaN HEMT with NCD heat spreading films.

mask. An SEM micrograph of the etch NCD region can be viewed in Fig. 3.11. The SiO_2 film in the gate opening was etched using dilute HF (10:1, 30 sec.) to minimize plasma damage and an e-beam evaporated Ni/Au (20/200 nm) gate electrode was lifted off. The continuity of the gate metal over the 0.55 μm thick step was verified using SEM imaging (see Appendix I). Control samples with and without NCD films were fabricated for comparison.

3.2.2.2 DC Bias Raman Thermography

Device temperature profiling was performed using Raman thermography [13, 109]. This spectroscopic technique measures the shift in the Raman transverse optical (TO) phonon mode peak position that is caused by temperature-dependent

phonon scattering. The 532 nm laser line of a Roithner DPSS diode-pumped solid-state laser (RLTMGL-532-200) was focused through a 50x, 0.55 NA Mitutoyo objective onto the sample. Raman scattered light was collected through the same objective and focused through a 100 μm diameter fiber into an Ocean Optics QE65000 thermoelectrically cooled CCD spectrometer. The temperature-dependent shift in the device temperature was calibrated by first placing the samples on a heated chuck and determining the corresponding Raman shift at a given temperature. Following the calibration, the approximately 1 μm diameter laser spot was focused into the 20 μm long gate-drain region spacing, and the devices were biased at V_{GS} such that I_{DS} was about 5 mA (V_{GS} was about -1 V). The drain bias was increased from 0 to 200 V to yield DC operating power range of 0 to 10 W/mm (device width was 100 μm). For each device, three measurements were averaged for each operating condition measured. The shift in the GaN TO (568 cm^{-1}) and Si (521 cm^{-1}) Raman modes were recorded under these bias conditions and the Raman peak position was used to determine the corresponding device temperature in these two material layers. The extracted device temperature as a function of device power is reported in Fig. 3.12. Percent change in device temperature is given in Table 3.4.

Table 3.4: Improvement of device operating temperature of AlGaN/GaN HEMTs with and without NCD heat spreading films.

P_{Ctrl} (W/mm)	$T_{CH,Ctrl}$ (℃)	P_{NCD} (W/mm)	$T_{CH,NCD}$ (℃)	T_{CH} % change
0	68.74	0	56.18	18.27
0.51	79.24	0.50	57.88	26.96
2.35	84.92	2.39	68.01	19.91
5.34	96.56	5.83	76.0	21.29
8.13	93.49	9.3	79.05	15.44

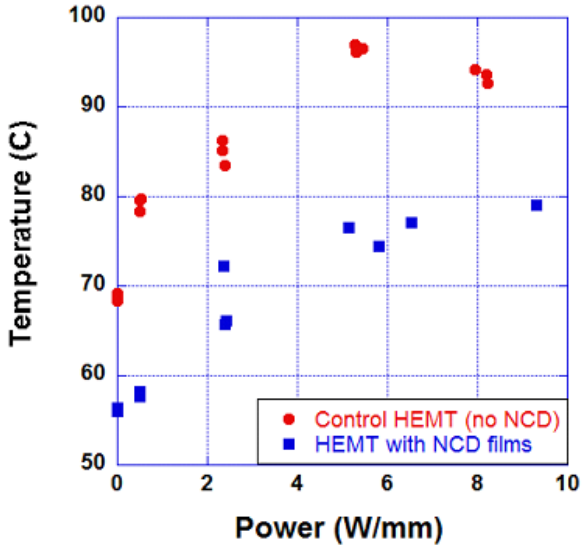

Figure 3.12: Raman thermography profile of the device channel temperature of AlGaN/GaN HEMTs with and without NCD heat spreading films.

While the device temperature could be further reduced using a SiC substrate, we have restricted the substrate to one with a lower thermal conductivity (κ=130 W/m-K for Si vs 370 W/m-K for 4H-SiC) in order to channel heat flow through the diamond films [1]. Fabrication on sapphire substrates (approximately 33 W/m-K at 300 K) was not feasible due to NCD film exfoliation caused by the large tensile stress created during cooldown after NCD growth.

3.2.2.3 Electroluminescence Profile

Images of the electroluminescence emission from the NCD-capped HEMT, as well as the reference HEMTs with and without SiO_2 passivation, were taken using a LN_2-cooled CCD camera. No optical filters were used, so the images depict the

entire spectral range of the CCD camera (200-1100 nm). Details of the EL imaging are given in Ref. [110]. The HEMT devices were biased in the on state with V_{DS} = 200 V (I_{DS} = 12 mA), V_{GS} = 1 V.

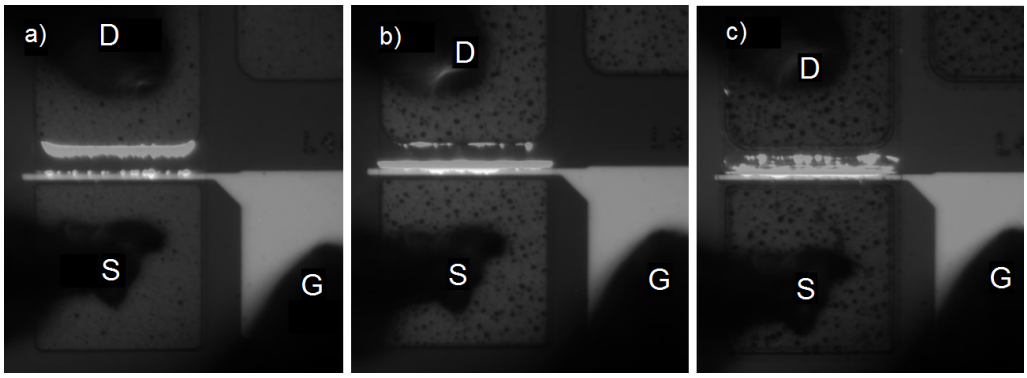

Figure 3.13: Broad spectrum (no filters used) EL images of the a) reference, b) SiO_2-passivated, and c) NCD-capped HEMT devices, measured at V_{DS} = 200 V, V_{GS} = 1 V, and I_{DS} = 12 mA.

The devices imaged had a gate-drain spacing of 15 μm, and the EL emission was observed from within that region. On the reference sample (Fig. 3.13a), most of the EL emission originated near the drain pad, whereas on the SiO_2 capped HEMT without NCD most of the EL emission was observed near the gate pad. This phenomenon is discussed in detail in Chapter 4, where different passivation techniques are explored. The EL profile of the NCD-capped HEMT exhibited significant emission in the gate-drain spacing, possibly due to hot electron detrapping from defect levels in the NCD layer.

3.2.2.4 Electrical Characterization

Hall measurements on a Van der Pauw test structure were performed before and after NCD deposition. Two Van der Pauw structures, shown on the top right hand corner of Fig. II.1 in Appendix II, were designed: one where the active region was shielded from the NCD recess etch and another one that was not. Therefore, Hall measurements performed after NCD etching could determine the effect of the NCD etch on the HEMT parameters.

The Hall measurements before NCD etching yielded R_{SH} = 563 Ω/sq., sheet carrier concentration n_S of 6.8x10^{12} cm^{-2}, and Hall mobility μ_h of 1507 cm^2/V-s at room temperature. Post-diamond etch measurements resulted in n_S=5.7x10^{12} cm^{-2}, μ_h=399 cm^2/V-s, R_{SH}=2860 Ω/sq., and ρ_C=9.5x10^{-3} Ω-cm^2 (31 Ω-mm). However, the post-diamond etch measurements from the protected Hall structure were consistent with the data measured prior to diamond etching. Therefore, the decrease in mobility and sheet carrier density was due to plasma damage, not thermal damage, which is consistent with the results presented in Section 3.1.

Table 3.5 lists the changes in saturation drain current I_{DSS} (I_{DS} at V_{DS} = 5 V, V_{GS} = 0 V), transconductance G_m, threshold voltage V_{TH}, and on resistance R_{ON}. Figure 3.14 presents the I-V characteristics of the diamond HEMT.

Table 3.5: Device parameters on control sample, after SiO_2 deposition, and after NCD deposition.

HEMT	I_{DSS} (mA/mm)	$G_{m,SAT}$ (mS/mm)	V_{TH} (V)	R_{ON} (Ω-mm)
Control	123	122	-1.92	19.2
SiO_2 cap	191	152	-2.03	14.7
SiO_2 and NCD cap	143	107	-2.22	18.0

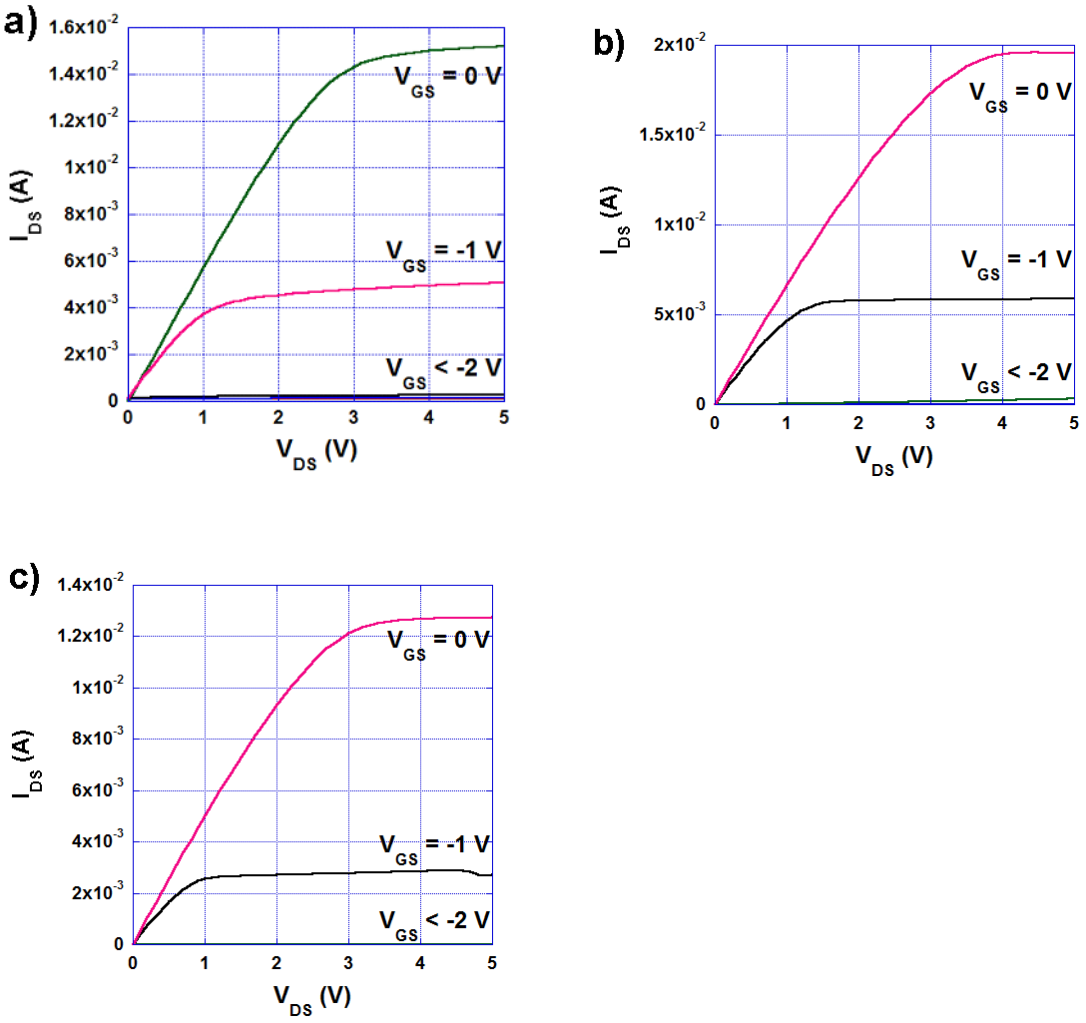

Figure 3.14: Current-voltage characteristics of an AlGaN/GaN HEMTs: a) with NCD heat spreading films, b) with SiO_2 passivation but without NCD heat spreading films, and c) a reference HEMT with no SiO_2 passivation and no NCD heat spreading films.

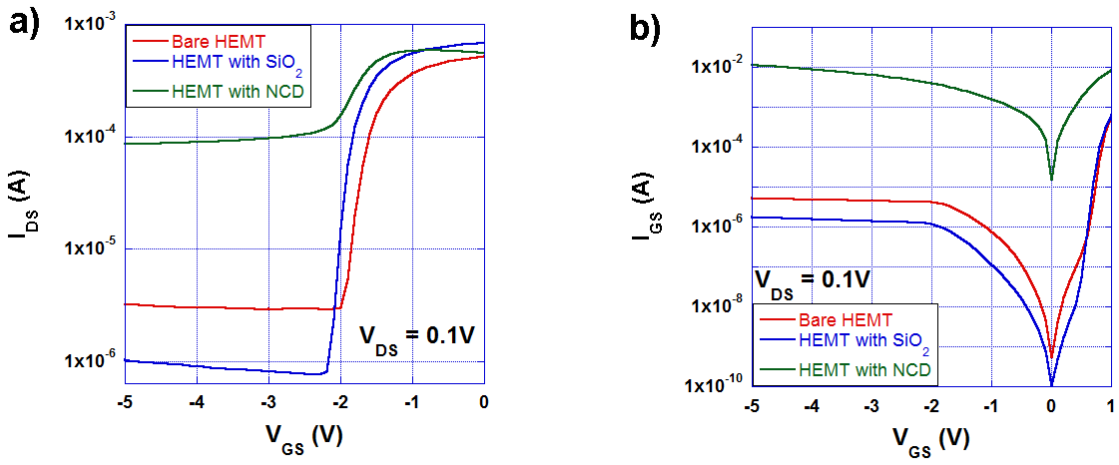

Figure 3.15: a) Drain current and b) gate current vs. gate voltage at $V_{DS} = 0.1$ V for the three samples.

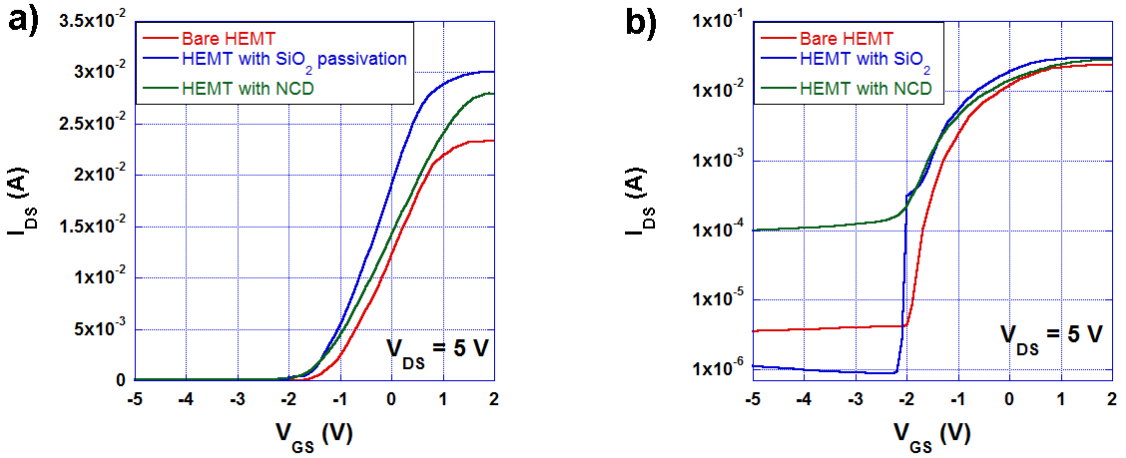

Figure 3.16: Drain current vs. Gate voltage at Vds = 5 V for the three samples on a) linear and b) semilog scale.

Following the NCD film deposition, the isolation current between devices increased significantly, from the nA to the mA range, as could be seen in the previous section. This leakage current did not decrease if undoped NCD was deposited instead, and was therefore attributed to surface leakage, either due to a Ga-rich GaN surface resulting from N desorption during NCD growth, or to an NCD bottom surface accumulation layer due to the negative electron affinity of H-terminated NCD [1]. Another consequence of diamond surface leakage was the increase in off-state leakage by two orders of magnitude from 10^{-6} to 10^{-4} A (Fig. 3.15 and Fig. 3.16). Negative shift in threshold voltage indicated positive charge in the diamond layer separate from the positive charge usually found in PECVD SiO_2. Degradation in SiO_2 quality due to extended thermal exposure during diamond growth was mitigated by the NCD layer acting as a cap during growth. Alternative dielectrics such as PECVD SiN_x and ALD Al_2O_3 were also used as NCD nucleation layers, however device modulation was achieved only with SiO_2. Even though the Schottky gate was formed after NCD deposition, the Schottky barrier height decreased by about 50 %, and the gate ideality factor increased five-fold.

Breakdown voltage measurements were performed on all three samples, and an additional reference sample with SiN_x passivation (no diamond). It can be seen in Fig. 3.17 that while the SiN HEMT has the highest breakdown voltage (560 V) due to its high dielectric constant (7.5 for SiN as opposed to 3.9 for SiO_2), its feasibility for a diamond nucleation substrate was limited. The breakdown voltage of the NCD HEMT was lowest (140 V) with very high off-state current leading up to it. The SiO_2 and bare HEMT samples had comparable breakdown voltage of about 210 V.

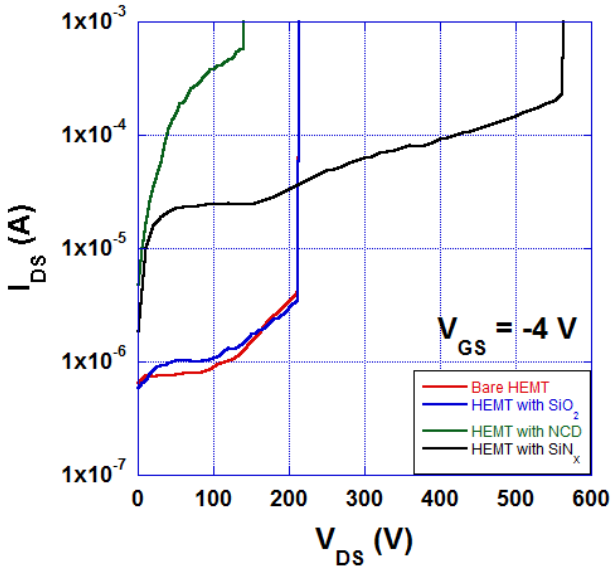

Figure 3.17: Breakdown voltage of HEMT devices with and without diamond and with different passivation layers.

The 50 nm dielectric thickness represented a trade-off between providing maximum heat spreading benefit and reducing the diamond-HEMT leakage current. Simulations of the effect of oxide thickness on device temperature have been performed by Feygelson et al. The oxide thickness was varied between 10 and 300 nm. At 50 nm, the power required to increase the device temperature by 100 ℃ decreased from 5.2 to about 2.5 mW, i.e., the benefit of the diamond was reduced by about 50 %. [111]

3.2.2.5 Temperature Dependent Electrical Characterization

High temperature characterization was performed on a reference (non-capped), SiO_2-capped, and NCD-capped HEMT. Room temperature parameters are listed in Table 3.6.

Table 3.6: Parameters of bare, SiO_2-capped, and NCD-capped HEMTs tested in this section.

HEMT	I_{DSS} (mA/mm)	$G_{m,SAT}$ (mS/mm)	V_{TH} (V)	R_{ON} (Ω-mm)
Control	123	104.5	-1.79	19.7
SiO_2 cap	176	145.5	-2.02	15.5
NCD cap	157	113.9	-2.13	12.6

R_{ON} (Ω/sq.)	μ_{HALL} (cm^2/Vs)	N_{SH} (cm^{-3})	R_C (Ω-mm)	$\rho_{C,SP}$ (Ω-cm^2)
607	1500	$6.87x10^{12}$	0.59	$5.45x10^{-6}$
563	1510	$7.35x10^{12}$	0.52	$5.75x10^{-6}$
505	1470	$8.42x10^{12}$	0.94	$2.5x10^{-5}$

Open gated (V_{GS} = 0 V) I_{DS}-V_{DS} characteristics of the HEMTs and I_{DS}-V_{DS} curves of the NCD-capped HEMT are presented in Fig. 3.18. The decrease in saturation drain current I_{DSS} and transconductance G_m after NCD growth (Table 3.6, Fig. 3.20) occurred due to a reduction in pinch-off voltage V_P following the increased drain-gate coupling through the SiO_2 and NCD films. This reduction in V_P is also evident at elevated temperatures in Fig. 3.18b. Table 3.6 and Fig. 3.21 show a decrease in the on-resistance R_{ON}, due to improved sheet resistance R_{SH} and sheet carrier density N_{SH} without sacrificing mobility, as measured by the Van der Pauw and transfer length methods, which indicated additional tensile strain on the III-Nitride structure. Apart from maximizing the NCD film effectiveness, the thickness of the SiO_2 layer was limited by a threshold voltage shift of -4.6 mV/nm of

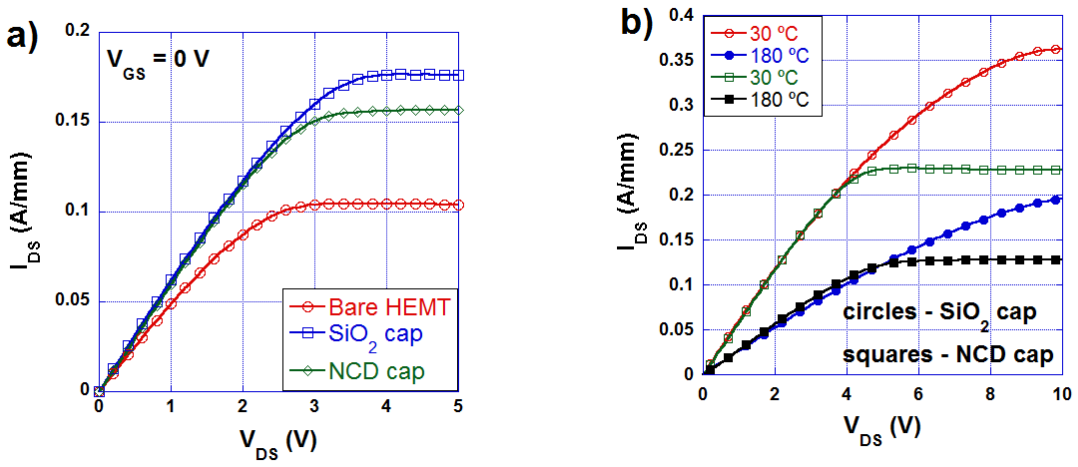

Figure 3.18: I_{DS}-V_{DS} (V_{GS} = 0 V) characteristics of HEMTs with SiO_2 and NCD cap a) compared to a bare HEMT at room temperature and b) as a function of temperature.

deposited SiO_2, as opposed to -0.22 mV/nm of NCD. Linear reduction in normalized I_{DSS} (Fig. 3.20b) and linear increase in normalized on-resistance R_{ON} with temperature (Fig. 3.21b), combined with low V_T dependence on temperature (Fig. 3.19), meant the current was limited by the electron saturation velocity at high temperatures.

To illustrate the benefits of NCD thin film incorporation in power switching HEMT devices, we have tabulated the effect of reduced R_{ON}, as measured in Fig. 3.21a, over the reduced device operating temperature measured using Raman thermography. Using this approach, we can calculate the reduction of conduction losses of the boost converter circuit shown in Fig. 7.1. The results are shown in Table 3.7. $R_{ON,NCDcap}$ decreased from $R_{ON,Ctrl}$ based on the average of 20.37 % lower

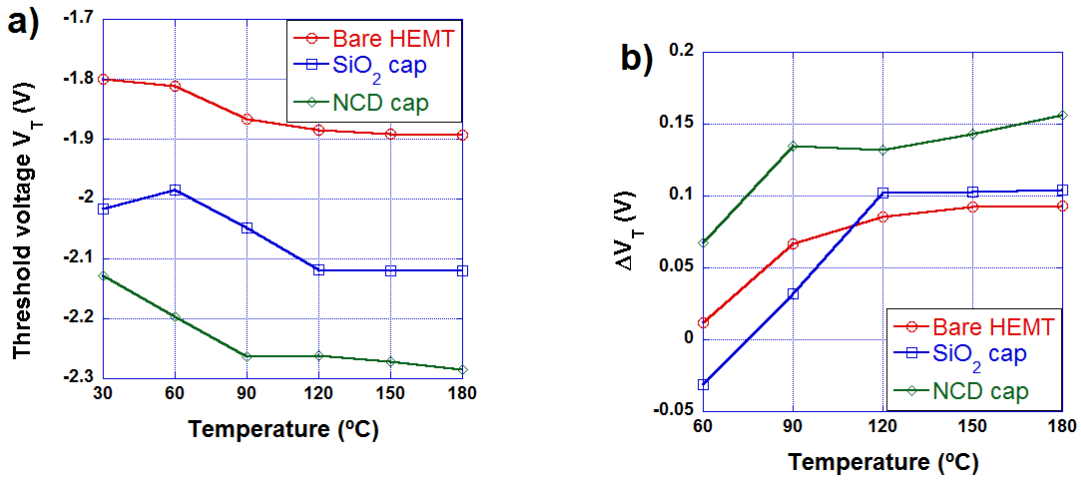

Figure 3.19: a) Threshold voltage V_T and b) change in threshold voltage ΔV_T of HEMTs as a function of temperature for a bare, SiO_2-capped, and NCD-capped HEMT..

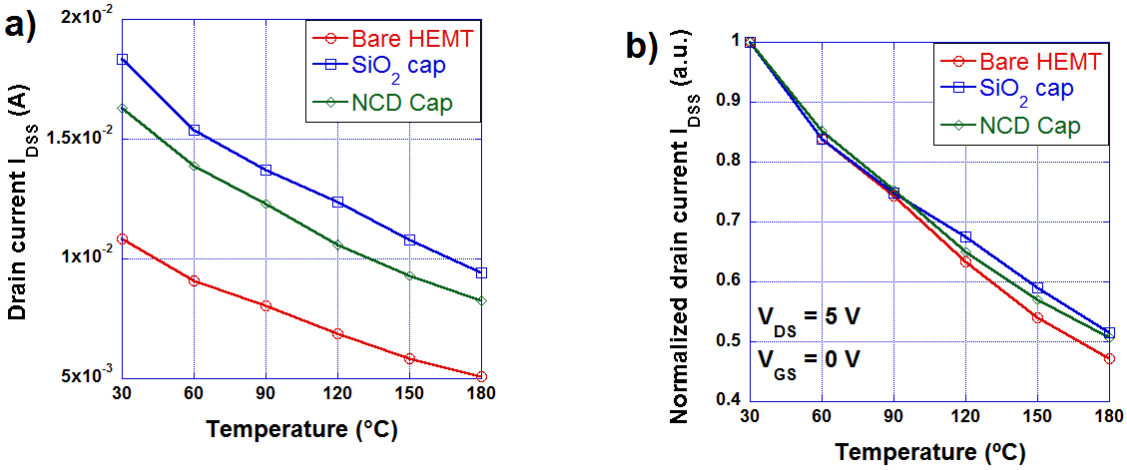

Figure 3.20: a) Absolute and b) normalized saturation drain current I_{DSS} (V_{DS} = 5 V, V_{GS} = 0 V) as a function of temperature for a bare, SiO_2-capped, and NCD-capped HEMT.

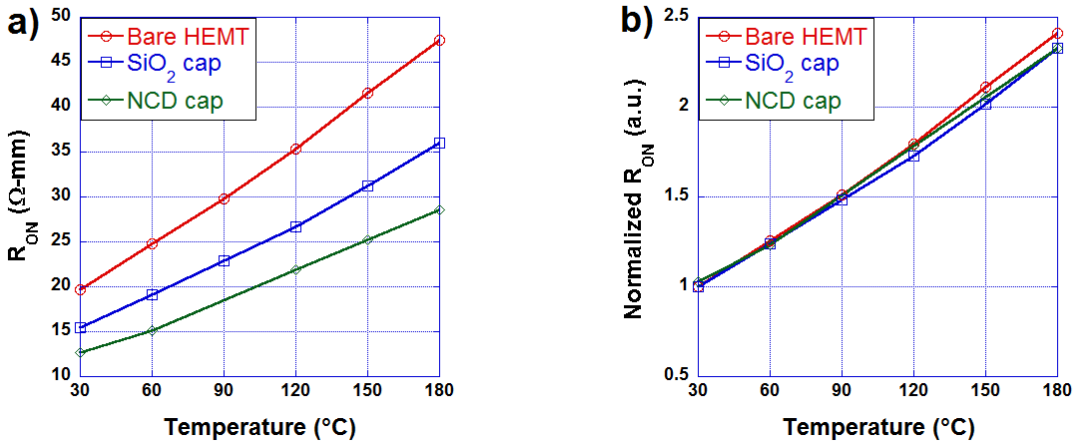

Figure 3.21: Temperature dependent a) absolute and b) normalized on-resistance R_{ON} for a bare, SiO_2-capped, and NCD-capped HEMT.

device operating temperature measured in Table 3.4. This effectively moves the R_{ON} operating point to the left on the curves in Fig. 3.21, and as a result NCD-capped devices operate with approximately 10.24 % lower on resistance. The addition of a SiC substrate furthers the thermal benefit on the on resistance, reducing it by further 19.55 %. $R_{ON,SiCsub}$ combines the effect of NCD thin film incorporation and a SiC substrate, and together with the corresponding values of the drain current yields the HEMT conduction losses in the on state ($P=I^2R$). The average reduction in conduction loss over the measured temperature range was 31.73 %, with about a third of this contribution due to the growth of the 0.5 μm thick NCD cap.

Boost converters currently represent a state of the art benchmark for evaluation of HEMT-based power switching applications [112, 113]. In a boost converter, overall circuit efficiency can reach up to 98 %, with values of 95 % routinely reported

Table 3.7: On resistance based analysis of conduction loss reduction in NCD cooled HEMT devices.

T_{meas} ℃	$R_{ON,Ctrl}$ (Ω-cm^2)	$R_{ON,NCDcap}$ (Ω-cm^2)	$R_{ON,SiCsub}$ (Ω-cm^2)
68.74	4.65	4.22	3.39
79.24	4.98	4.47	3.60
84.92	5.15	4.62	3.71
96.56	5.51	4.90	3.94

Legend:
T_{meas} – Raman thermography measured temperature range of control device.
$R_{ON,Ctrl}$ – R_{ON} of control device in the T_{meas} range.
$R_{ON,NCDcap}$ – reduction of R_{ON} by NCD film incorporation.
$R_{ON,SiCsub}$ – reduction of R_{ON} by addition of NCD films and SiC substrate.

T_{meas} ℃	$I_{DS,Ctrl}$ (mA)	$I_{DS,Ctrl,NCD}$ (mA)	$P_{CL,Ctrl}$ (mW)	$P_{CL,Ctrl,NCD}$ (mW)
68.74	5.16	5.00	5.41	3.71
79.24	4.91	4.77	5.24	3.58
84.92	4.77	4.64	5.13	3.50
96.56	4.50	4.39	4.87	3.32

Legend:
$I_{DS,Ctrl}$ – I_{DS} corresponding to $R_{ON,Ctrl}$ (V_{DS}=1 V, V_{GS}=0 V).
$I_{DS,Ctrl,NCD}$ – I_{DS} corresponding to $R_{ON,SiCsub}$.
$P_{CL,Ctrl}$ – Conduction power loss for I_{DS}.
$P_{CL,Ctrl,NCD}$ – Conduction power loss for $I_{DS,Ctrl,NCD}$.

even when Si power MOSFET were used. The losses are split almost equally among power switch losses (consisting of on-state conduction and switching losses in the HEMT), losses in the passive elements (inductor and capacitor), and losses in the Schottky diode. HEMT conduction losses in the off state are typically minimized by optimal buffer layer growth conditions and surface passivation techniques. Wu et al. measured a total of 0.82 % of input power P_{IN} lost in the HEMT (0.55 % due to conduction losses), 0.68 % of P_{IN} lost in the passive components (mainly the inductor), and 0.7 % of P_{IN} lost in the SiC Schottky diode. The switching loss at low switching frequencies is negligible, and both Wu and Saito reported almost equal

conduction and switching losses in the 1.2-1.5 MHz range. Our analysis here resulted in about 10 % reduction in conduction losses as a result of the improved R_{ON} due to NCD incorporation and reduced device operating temperature. A reduced R_{ON} also decreases the switching loss, and thus we could conservatively assume that total HEMT losses could be reduced by about 15 % over a typical range of operating frequencies (0.5 to 1 MHz). For a 97 % efficient boost converter with total HEMT power loss of 1 %, this translates to a 0.15 % improvement in efficiency, or a 5 % reduction in total converter losses. In addition, the reduced operating temperature of the HEMT device would ease the overall thermal system designs specifications.

3.3 Chapter Summary

By incorporating NCD thin film growth prior to HEMT gate deposition, we have successfully demonstrated the reduction of device temperature at power levels up to 10 W/mm. Even though thermal applications remain a primary target, CVD diamond provides additional device engineering benefits due to its transparency in the UV range, wide band gap, susceptibility to p-type doping, and ability to form heterojunctions with other wide band gap materials such as 4H-SiC [114]. CVD diamond is a promising material for device integration, and further advances in processing technology could enable its use not only for heat spreading, but also for mechanical robustness and device substrate use [115].

The importance of the dielectric in nanocrystalline diamond HEMT devices in providing a nucleation layer, surface passivation, and gate insulation necessitated

further research in the area. Some of the highest quality dielectrics are grown using CVD. In the next chapter, we present a comparative study of AlGaN/GaN HEMT surface passivation using *ex-situ* and *in-situ* deposited SiN_x.

Chapter 4

Surface Passivation Comparison using in-situ and ex-situ deposited SiNx on AlGaN/GaN HEMTs

4.1 Introduction

Power switching devices require high breakdown field, low on-state resistance, stable operation under high channel temperatures, and low gate and drain leakage currents. GaN has been a promising material for high electron mobility transistor (HEMT) based power converters due to its wide band gap, high critical field, and high two-dimensional electron gas (2DEG) mobility [72, 113, 112]. However, one of the main performance limiting factors has been the high gate and off-state drain leakage currents in the transistor that are introduced by SiN_x passivation [116]. While microwave HEMT applications have traded off the increased leakage cost of SiN_x passivation for its well known benefit of reduced current collapse effects [9, 65, 66], power switching applications have stricter requirements in order to achieve competitive efficiency and reliability.

In this study, we demonstrate some key differences between *ex-situ* and *in-situ* SiN_x passivation. Traditionally, surface passivation of AlGaN/GaN HEMTs has been performed using a thin plasma-enhanced chemical vapor deposition (PECVD) SiN_x layer [67, 117]. Here, we refer to this SiN_x deposition as being performed

ex-situ. Chevtchenko *et al.* have demonstrated reduced reverse leakage current in GaN Schottky diodes passivated *ex-situ* by SiN_x or SiO_2 [10]. More recently, *in-situ* SiN_x growth inside the metal organic chemical vapor deposition (MOCVD) chamber immediately following AlGaN/GaN growth has been demonstrated [118, 70]. Using about 15 nm of in-situ Si_3N_4, Germain *et al.* have demonstrated increased DC drain current densities and transconductance. This passivation technique may prove beneficial for the development of stable enhancement mode operation HEMT devices. Such normally-off operation has been demonstrated by Higashiwaki *et al.* [69] using *ex-situ* SiN_x and more recently by Anderson *et al.* [88] using a thin AlN capping layer.

Performing *ex-situ* SiN_x passivation increases the reverse gate leakage and off-state channel leakage by about three orders of magnitude. Electroluminescence (EL) images of AlGaN/GaN HEMT devices operating in forward blocking mode with up to 400 V drain bias demonstrates reduced channel emission profiles of *in-situ* passivated devices. Reduced channel temperature on *ex-situ* SiN_x-passivated devices correlates with reduced EL emission profiles compared to non-passivated reference samples. Photoluminescence (PL) spectra indicate reduction of nonradiative recombination centers, indicating lower surface state density and thus better passivation using the *in-situ* SiN_x approach. The thickness of the *in-situ* SiN_x layer was determined using transmission electron microscopy (TEM) and capacitance-voltage measurements.

4.2 Experimental Details

Three 25 nm $Al_{0.25}Ga_{0.75}N$ / 2 μm GaN HEMT devices were fabricated using no passivation layer (sample A), passivation with 100 nm PECVD SiN_x deposited *ex-situ* after gate metal deposition (sample B), and passivation using a 30 nm thick *in-situ* SiN_x layer grown in the MOCVD chamber immediately after AlGaN and GaN growth (sample C). Sample A and B were grown using MOCVD on a-plane sapphire substrates with an AlN nucleation layer, and sample C was grown on an n^+ 4H-SiC substrate. PECVD SiN_x growth was performed using a 23.5/20/980 sccm $SiH_4/NH_3/N_2$ atmosphere at 300 ℃, 650 mT pressure, and 20 W HF/LF power at 62 % duty cycle. The *in-situ* SiN_x on sample C was grown using a 0.1 % SiH_4, NH_3, and N_2 atmosphere at 1050 ℃ and 50 Torr pressure, resulting in about 2 nm/min SiN_x growth rate.

Fabrication commenced with a 100 nm deep mesa isolation etch using a Cl_2/Ar-based ICP process (10/5 sccm Cl_2/Ar, 150 W ICP, 40 W RIE, 160 V DC bias, 5 mT). Following the Ohmic contact lithography, samples A and B were cleaned in O_2 plasma for 2 minutes (50 W, 0.9 Torr). Sample C had the *in-situ* SiN_x etched in SF_6 plasma for 1 minute (26 sccm SF_6, 44 W RIE, 50 mT), after which the 50 W O_2 plasma clean was performed. This etch was done for consistency with the structure of samples A and B. According to Van Daele *et al.*, the *in-situ* SiN_x etch does not influence the contact resistance. Rather, when the SiN_x was not etched, the Ohmic contact conduction mechanism switched from Ti-based to Al-based [71].

A 20 nm Ti/80 nm Al/40 nm Ni/50 nm Au Ohmic metal stack was deposited

using e-beam evaporation and was rapid-thermal annealed for 30 sec at 900 ℃. Using the transfer length method (TLM), we obtained a specific contact resistivity of ρ_C = 4.4x10^{-6} Ω-cm^2 (0.71 Ω-mm) on samples with a sheet resistance of 1129 Ω/sq. Hall probe measurements yielded a sheet density of 2.9x10^{12} cm^{-2} and mobility of 1099 cm^2/Vs, which were typical values for the samples used in this study.

Fabrication of samples A and C was completed after the deposition of Ni/Au gate metal stacks. Sample B had 100 nm PECVD SiN_x deposited after the Ni/Au gate. The SiN_x was then patterned and etched from the regions of the Ohmic contacts and a Ti/Pt/Au overlay metal was deposited. It should be noted that the Ni/Au metal stacks on samples A and B acted as Schottky gates, whereas sample C had an MIS gate due to the presence of the *in-situ* SiN_x underneath the Ni/Au. Schematics of all samples are presented in Figure 4.1.

In addition to electrical characterization, electroluminescence (EL) imaging using a LN_2-cooled CCD camera was performed on all three samples. Details about the EL imaging technique can be found elsewhere in the literature [110]. No optical filters were used, so the images depict the entire spectral range of the CCD camera (200-1100 nm). Photoluminescence spectroscopy was performed at room temperature using an Ar-ion laser (excitation power of 40 mW, spot size < 1 μm), operated in single line mode, emitting the 351 nm line. The EL was collected through an optical fiber and was detected via an Ocean Optics HR-4000 spectrometer using a 10 ms integration time, averaged 64 times.

Raman thermography was performed using a technique described by Simms *et al* [13, 119]. The 532 nm laser line of a 150 mW Roithner DPSSL-Series doubled

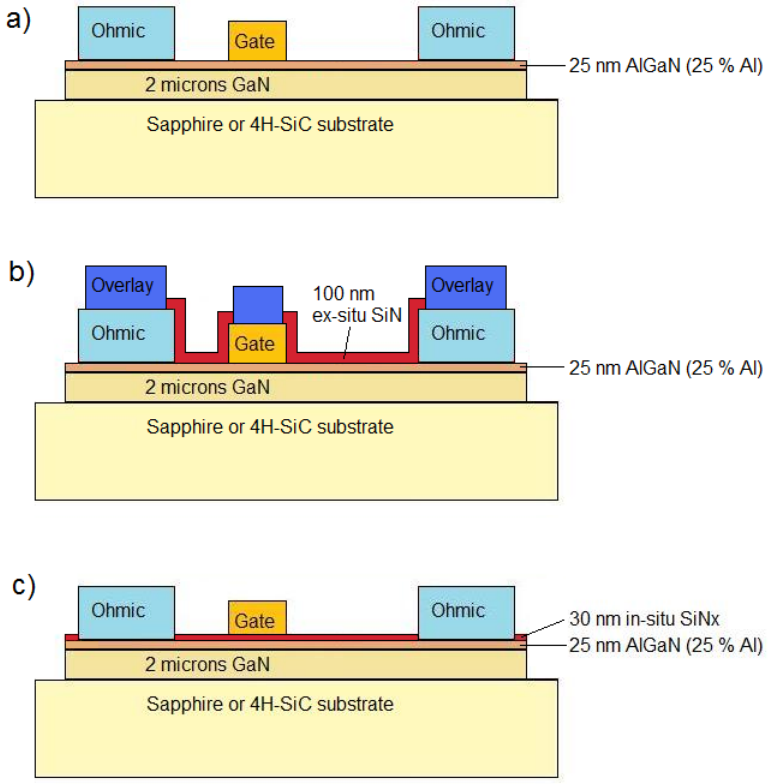

Figure 4.1: Schematic representations of the fabrication processes for a) an ex-situ SiN_x-passivated HEMT (sample B) and b) an in-situ SiN_x-passivated HEMT (sample C).

Nd:YAG laser was focused into the gate-drain region of the samples. The Raman spectra were collected through a 50x, 0.75 NA objective and focused on the detector array of an Ocean Optics QE65000 spectrometer through a fiber optic. It has been shown in the literature that increases in the temperature lead to reductions in the Raman shift position [120, 121]. This phenomenon may be used to measure the local temperature within a given material following calibration of the measured shift to a known sample temperature. Thermal calibration was performed by heating the

samples on a hot chuck, allowing the sample and the chuck to equilibrate, and then measuring the corresponding Raman spectra from the HEMT structure. Following the calibration, Raman spectra were collected under various bias conditions and the temperature of the HEMT channel was determined based on the shift in the Raman line. The devices used in this study all had 5 μm gate lengths and 15 μm gate-drain spacings. Measurements of the channel temperature were performed in the active region of approximately equal distance from the gate and the drain.

4.3 Results and Discussion

Current-voltage measurements of sample B before and after SiN_x passivation are presented in Figure 4.2. The curves were measured using an HP4145B semiconductor parameter analyzer. The reverse gate current ($I_{G,REV}$) and the off-state drain current ($I_{DS,OFF}$) were measured on Sample B before and after *ex-situ* SiN_x deposition. It was observed that the *ex-situ* SiN_x deposition induced about three orders of magnitude increase in $I_{G,REV}$ and $I_{DS,OFF}$. The increase in $I_{DS,OFF}$ was significant enough to influence the device characteristics in forward blocking mode as well (Figure 4.3, $V_{DS} > 4.5$ V, $V_{GS} < -1$ V). Such increases would not only decrease the efficiency of power converters containing these devices due to increased off-state loss, but may also be deleterious for their reliability. Specifically for the boost converter circuits demonstrated in Ref. 2 and 3, increases in $I_{DS,OFF}$ and $I_{G,REV}$ would reduce the current transferred from the inductor to the output capacitor, thus reducing the output power (P_{OUT}).

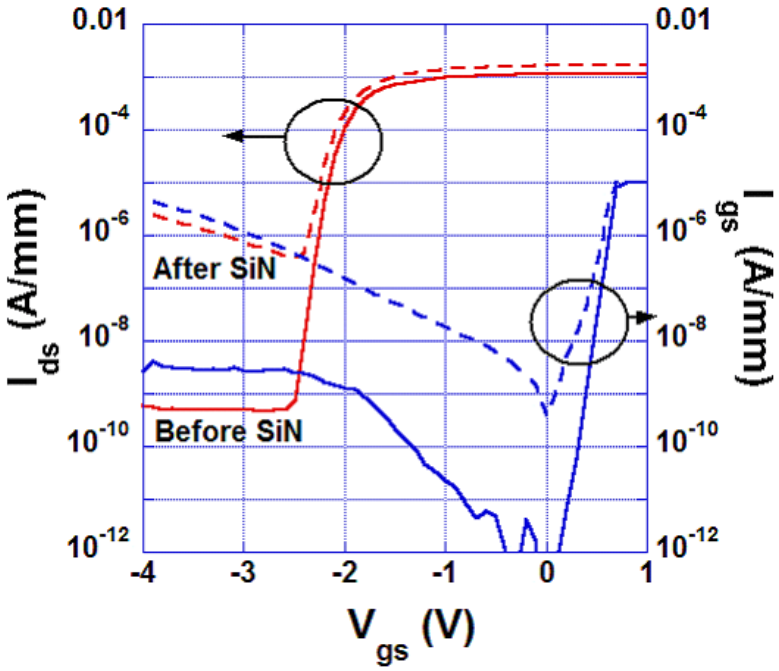

Figure 4.2: Drain and gate current as a function of gate voltage before (solid lines) and after (dashed lines) ex-situ SiN_x passivation of sample B.

Compared to the *ex-situ* SiN_X on sample B, the *in-situ* SiN_x growth on sample C resulted in a device exhibiting lower surface state density, as indicated in Figure 4.4 by the sharper slope of its C-V characteristics. The C-V characteristics were measured at 100 kHz from the gate metal to an adjacent Ohmic contact using a Keithley 590 LCR meter. For sample C, an accumulation capacitance (C_{OX}) of about 38.6 nF/cm^2 was measured and, using a SiN_x dielectric constant of 7.5, yielded a dielectric thickness t_{OX} of about 30 nm.

This result was confirmed using cross-section transmission electron microscopy (TEM), where bright-field imaging of the layers is presented in Figure 4.5. An ion-beam deposited Pt capping layer was used to protect the surface prior to focused

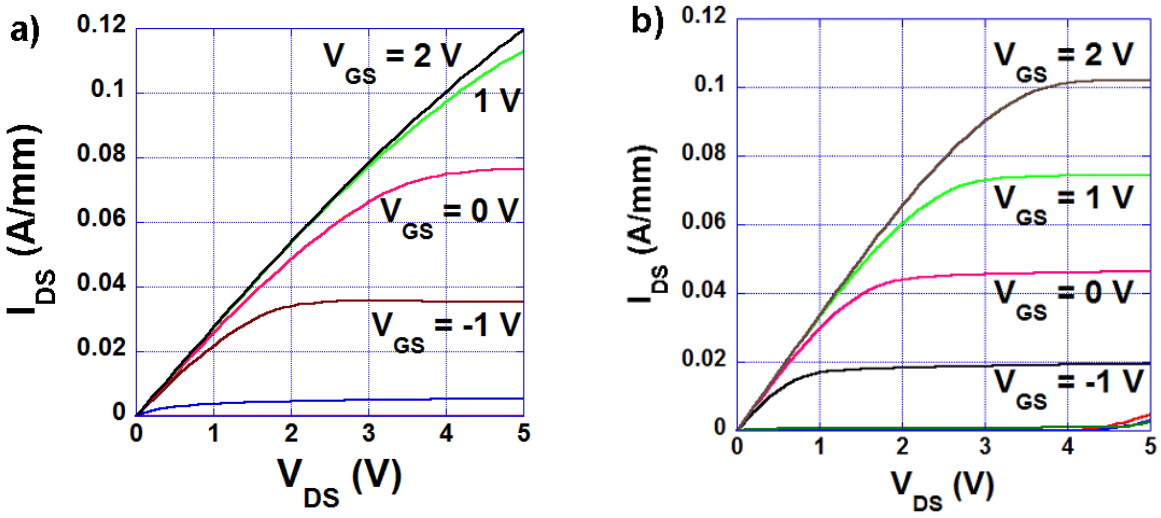

Figure 4.3: Current-voltage characteristics of the AlGaN/GaN HEMT a) before and b) after ex-situ SiN_x passivation (sample B).

ion beam cross-sectioning and subsequent lift-out. Considering that the gray layer in Figure 4.5 located between the bright *in-situ* SiN_x and the Pt layer could have resulted from the intermixing of the two materials during sample preparation, a total SiN_x thickness of about 30 nm was observed. Additionally, TEM also verified the desired 25 nm AlGaN layer thickness. Since AlGaN is atomically lighter than GaN, the layer would be expected to be lighter gray. However, the larger defectivity observed during bright-field TEM imaging conditions resulted in a dark AlGaN layer in Figure 4.5.

The C-V characteristics of samples B and C (Figure 4.4) had similar hysteresis of about 0.5 V, corresponding to approximately 10.4 nC/cm^2 negative charge in both SiN_x layers. However, using a Schottky gate on sample B created positive surface charge underneath the gate, which has been attributed by Saito *et al.* to N vacancies

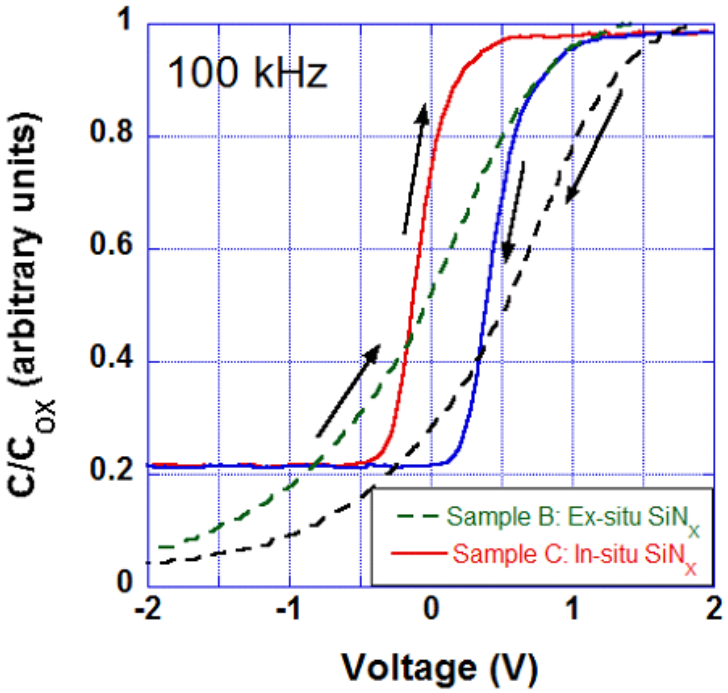

Figure 4.4: Normalized high-frequency capacitance-voltage characteristics of AlGaN/GaN HEMTs with in-situ and ex-situ SiN_x passivation (samples B and C).

created by plasma and thermal damage during processing.[4] This positive charge is believed to increase the reverse gate current by lowering the Schottky barrier height, ultimately increasing the off-state leakage of the device.

To better characterize the effects of increased device leakage currents, EL imaging was employed in the gate-drain area of the HEMT samples. Presented on Figure 4.6 are merged optical and EL images from the three samples, biased in forward blocking mode at V_{DS} = 350 V. The drain bias during EL imaging was limited by the breakdown of air between the probes. In the presence of a high dielectric constant liquid on the samples (e.g., Fluorinert^{TM}), we obtained

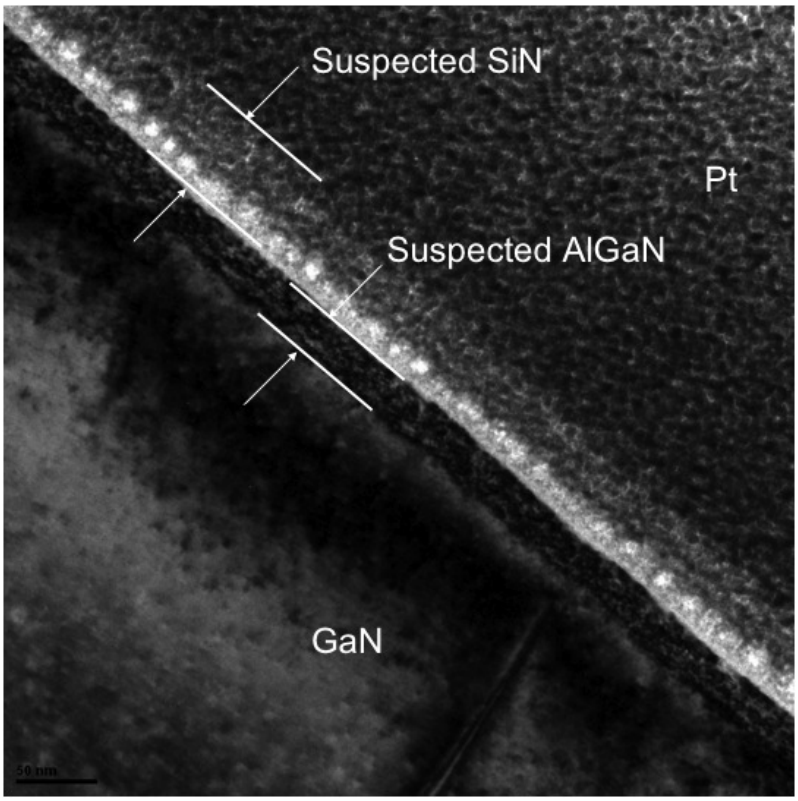

Figure 4.5: Cross-section transmission electron microscopy (TEM) image of the SiN_x/AlGaN/GaN interface of the AlGaN/GaN HEMT with in-situ SiN_x passivation (sample C). The gray layer in between the bright SiN_x and the Pt layers indicates a possible intermixing of the two materials due to sample preparation.

breakdown voltages in excess of 800 V.

Sample A (Fig. 4.6a) exhibited emission from the region of the drain pad adjacent to the channel, whereas the emission from sample B (Fig. 4.6b) was concentrated primarily inside the gate-drain spacing. Figure 4.6c shows that EL emission from sample C was concentrated on the gate pad, although a slight extension into the gate-drain region was observed. Due to the limited drain bias conditions in previously published EL studies ($V_{DS} < 100$ V), the channel emission from *ex-situ* SiN_x

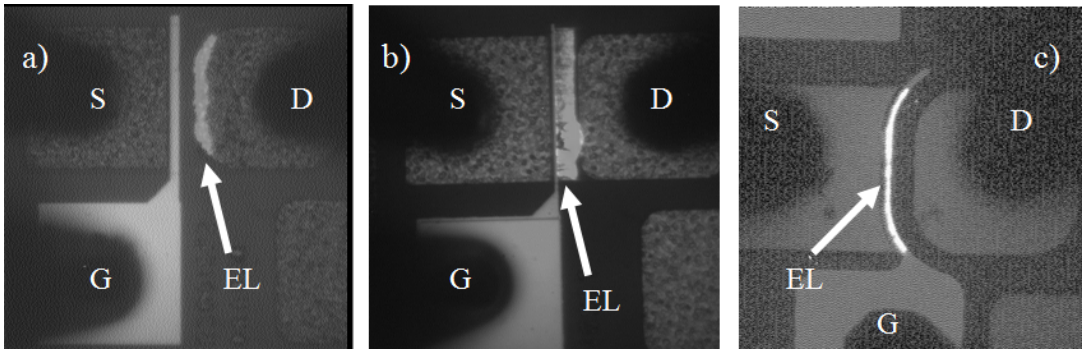

Figure 4.6: Optical images, overlaid with EL images (in bright white color), for the three samples: a) without passivation (sample A, V_{DS} = 350 V), b) with ex-situ SiN_x passivation (sample B, V_{DS} = 350 V), and c) with in-situ SiN_x passivation (sample C, V_{DS} = 400 V). All images were taken using a 10 second integration time.

passivated samples was observed near the gate pad [122–124]. Ohno *et al.* claimed that the presence of SiN_x eliminated the "virtual gate" caused by the presence of unpassivated surface states, thus shifting the peak channel potential from the drain to the gate region. Figure 4.7 clarifies the dependence of the channel emission on the drain field in the presence of *ex-situ* SiN_x (sample B). The EL images shown were taken at V_{DS} = 15 V, 200 V, and 400 V. It was clear that as the drain bias increased, EL was emitted from a larger portion of the channel, eventually extending to the drain region. Conversely, the spatial position of EL emission from sample C did not change location at lower V_{DS}. Therefore, maintaining the peak electric field near the gate even at high drain fields suggested improved surface passivation in the gate-drain region of sample C. For sample B, the presence of emission both near the gate and drain, seen on Figure 4.7a, suggested that the peak electric field

decreased near the drain and increased near the gate, an effect achieved in a similar fashion as using a field plate [73, 74].

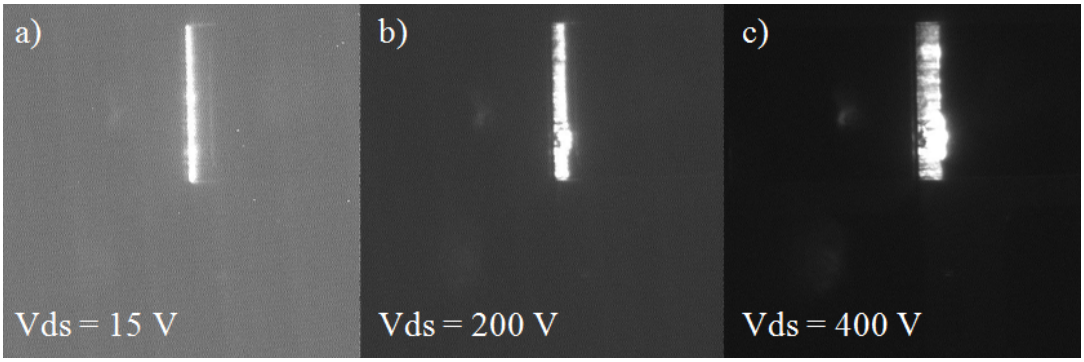

Figure 4.7: EL emission from sample B at a) V_{DS} = 15 V, 100 sec integration, b) V_{DS} = 200 V, 10 sec integration, and c) V_{DS} = 400 V, 10 sec integration. I_{DS} was maintained at approximately 1 mA under the three conditions.

While sample A may have emitted near the gate as well, the high intensity of the emission near the drain pad did not allow such emission to be observed on Figure 4.6a. The drain pad EL from sample A may have been partially caused by infra-red emission due to sample heating, the Gaussian tail of which may be detected by the CCD.

To better understand the origin of the EL emission, imaging was performed on the samples with a series of filters. Figures 4.8b and 4.8c show the EL response of sample A with an 830 nm low-pass filter and a 970 nm bandpass filter, respectively. It can be seen that most emission has a wavelength of less than 830 nm, which means it could originate either from defect levels in the III-Nitride (broad yellow luminescence), or the near IR range.

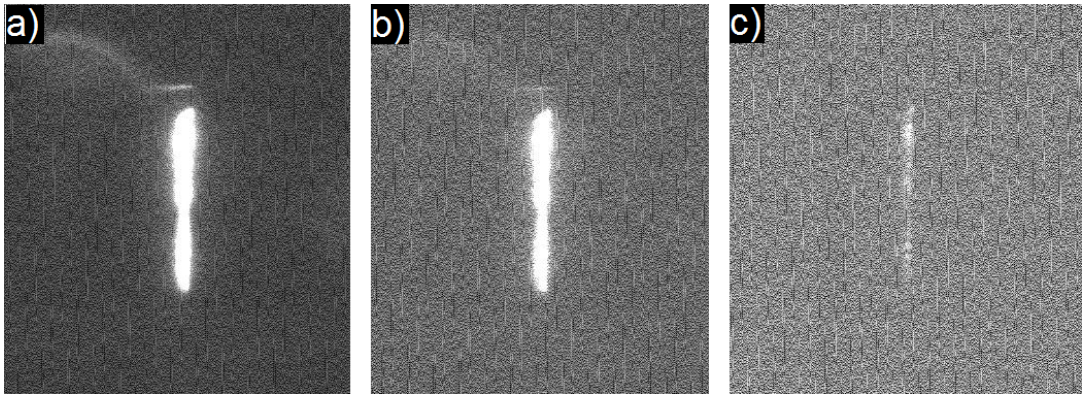

Figure 4.8: EL images of reference sample with a) no filter, b) 830 nm low-pass filter, and c) 970 nm bandpass filter.

Figure 4.9b-f shows EL images from sample C with bandpass filters in the 417-970 nm range. Each filter had an approximately 100 nm bandpass window. The emission was strongest with the 593 nm and 785 filters, indicating that emission in sample C originated from both the yellow and the near IR range. Samples A and B had similar behavior (images not shown for brevity). For sample A, we could speculate that the near IR emission near the drain pad was caused by self heating effects due to the high operating power during EL characterization. The broad yellow range luminescence originated from defect levels in the III-Nitride. One possible origin could be N vacancy related defects created during RTA annealing of the Ohmic contact. The fact that emission near the drain pad decreased significantly on samples B and C indicated that such defects may have been suppressed by the passivation process.

The hypothesis for the presence of near IR emission due to self-heating of sample A was further supported by the Raman thermography data, presented on

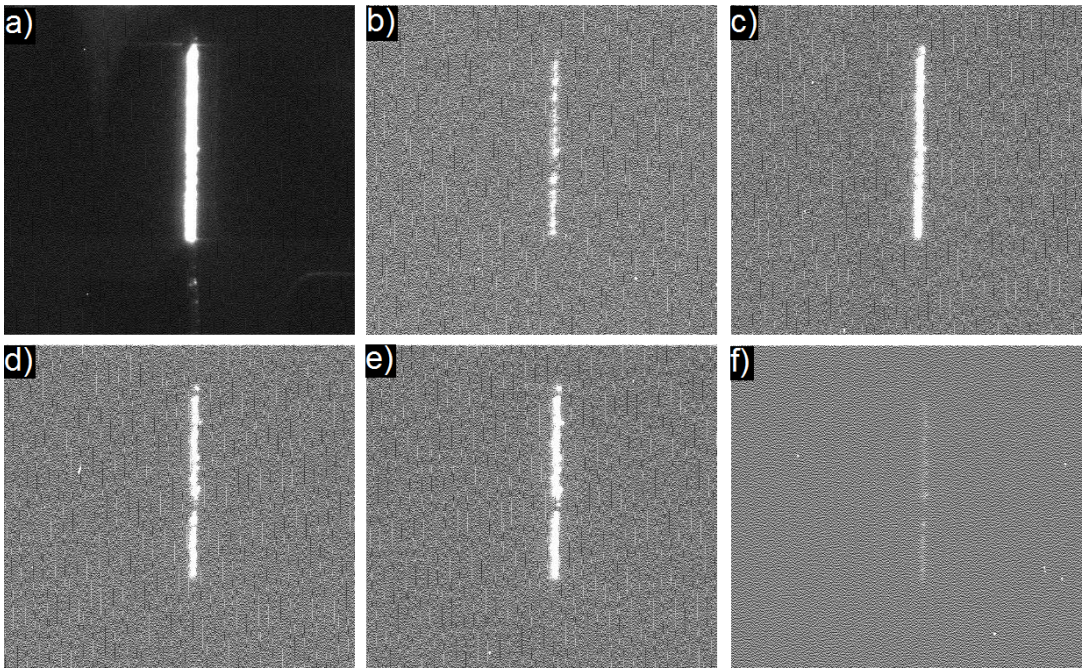

Figure 4.9: EL images of in-situ passivated sample with a) no filter, and b) 417 nm, c) 593 nm, d) 692 nm , e) 785 nm, and f) 970 nm bandpass filters.

Figure 4.10. The physical mechanism leading to the lower measured channel temperature on sample B is still under investigation, but it does correlate with the absence of emission from the drain pad when the sample was *ex-situ* passivated.

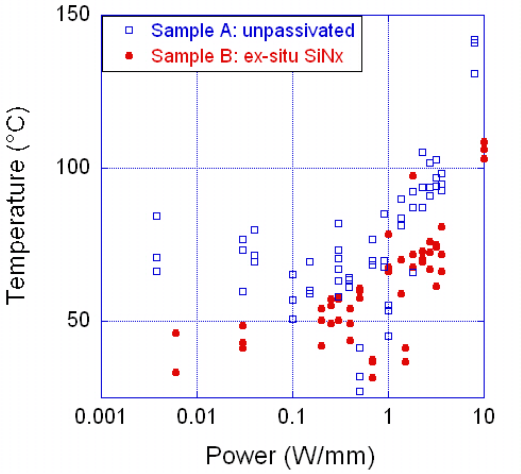

Figure 4.10: Channel temperature vs. device power level (drain current times drain voltage) measured using Raman thermography on samples A and B.

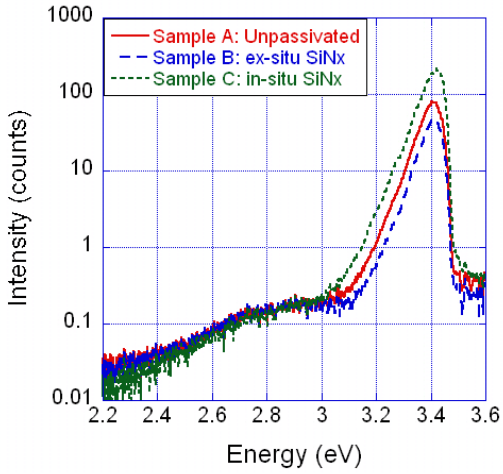

Figure 4.11: Photoluminescence spectra from the gate-drain region of all three samples studied.

The benefit of using *in-situ* SiN_x passivation was further illustrated by comparing the PL spectra from the three samples, measured at room temperature. Figure 4.11 shows that sample C exhibited the highest near-band edge luminescence, a result also observed by Xie *et al.* in their study of *in-situ* SiN_x nanonetworks [68]. We believe the higher PL intensity corresponded to the lowered density of non-radiative recombination centers at the SiN_x/AlGaN interface, which accounted for increased absorption on samples A and B. At the same time, yellow luminescence from the defect band of GaN was similar in intensity for all three samples, indicating

that the *in-situ* SiN_x did not introduce further defects into the active layers [125].

4.4 Chapter Summary

In this chapter, we have studied the differences in AlGaN/GaN HEMT surface passivation using *ex-situ* and *in-situ* SiN_x. We have shown that using *ex-situ* SiN_x degraded power switching performance due to the increased device off-state leakage and reverse gate leakage. The effect of the increased off-state drain current was further investigated using EL imaging, where emission from the gate-drain region was observed for *ex-situ* SiN_x. Using *in-situ* sample passivation increased the near band edge PL, helped to passivate surface states and nearly eliminated emission from the channel region. Combined with the low leakage MIS gate, *in-situ* SiN_x presents an ideal passivation material for next generation high voltage power switching applications.

Chapter 5

Characterization of Nanocrystalline Diamond Thin Films

5.1 Nanocrystalline Diamond Growth and Properties

Nanocrystalline diamond thin films have found a wide range of industrial applications. Machine tool coatings, AFM tips, MEMS devices, are just some examples where the unique properties of NCD have been applied. A primary advantage is the ability to grow such films on different substrates by applying a nucleation layer of diamond seed first. Seeding is best done in two ways. The substrate can be abrasively treated with diamond powder, which etches pits where diamond particles are trapped [126]. A gentler approach to surface treatment involves soaking the substrate in a diamond-ethanol suspension solution and applying an ultrasonic treatment to enhance particle adherence [127–129]. The diamond solution is produced using a detonation method, which produces diamond nanopowder with grain size of 4-10 nm [128–130]. The substrate surface is still somewhat damaged, but the seeding processes has proved crucial for nucleation of smooth NCD films. An improved nucleation process, aptly dubbed NNP (new nucleation process), has been proposed by Rotter in 1999 [131].

A modified NNP process, introduced by Philip et. al., is outlined below [132, 133]. The sample is cleaned in 4:1 H_2SO_4:H_2O_2 (piranha clean) for 10 min., followed by 10 min. in 1:1:5 NH_4OH:H_2O_2:H_2O (SC-1 clean), and finally etched in 37% HF

acid for 1 min. Subsequently, the sample is placed in the CVD reactor for 30 min. in a high methane atmosphere at 750 ℃, microwave power of 800 W, chamber pressure of 15 Torr, H_2/CH_4 flow rate of 900/7 sccm. Upon removal from the CVD reactor, the ultrasonic seeding process with diamond nanopowder in ethanol is performed for 30 min. Under the right conditions, seed density of 10^{12} cm^{-2} could be achieved. The higher the seeding density, the lower the NCD grain size will be after CVD growth, and the NCD film will have lower surface roughness. The sample is then blown dry with N_2, and brought back into the chamber for actual NCD growth, with RF power 1.5 kW at 2.45 GHz, at a dilute methane atmosphere. The growth rate is approximately 0.1 μm/hour and a nucleation density of about 7x10^{19} cm^2 is achieved. A trace amount of boron (about 1 ppm) is present in the reactor, which yields the NCD film unintentionally p-type doped. With intentionally added diborane, the NCD thin film will be p-type doped with hole concentration in the 10^{18}-10^{19} cm^{-3} range. We are also able to grow undoped NCD in a separate chamber to avoid boron contamination, producing NCD films with resistivity greater than 10^{10} Ωcm. The resulting NCD thin films were more than 99% sp^3-bonded, with 3.3 nm RMS thickness over a 1 μm^2 area [114, 134].

Table 5.1 lists some basic properties of NCD thin films grown by the process described above.

The UV transmission of our films matched closely to the values reported previously by Remes et al. [135]. The B-doped films had approximately 52% transmission at 351.0 nm, 58.8% at 363.8 nm (the two UV lines that were used for OBIC imaging) and 70.2% on average across the visible range. UV transmittance was higher for the

Table 5.1: Basic properties of NCD films grown using the modified NNP process [4].

Property	**Value for NCD**
Density (kg/m^3)	3,510
Young's modulus (GPa)	1120
Surface roughness (nm)	5-25
Grain Size (nm)	5-100
Thermal Conductivity (W/cm K)	13.70
Deposition Temperature (℃)	450-950
Sheet Resistance, undoped film	$>10^{13}$ Ω/sq.
Mobility, B-doped p$^+$ NCD (10^{17} cm^{-3})	10-90 cm^2/Vs
Mobility, B-doped p$^+$ NCD ($>10^{21}$ cm^{-3})	Superconducting at T<1.6 K

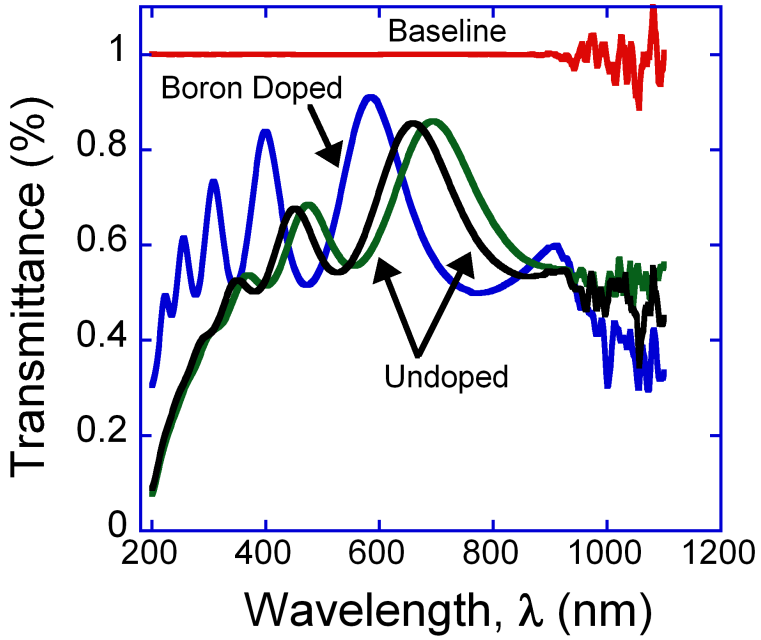

Figure 5.1: UV transmission spectra of the NCD films.

B-doped NCD samples than the undoped ones.

To identify the possible presence of deep trap levels in the NCD films, cathodo-luminescence (CL) studies were performed on NCD samples on Si substrates. The

CL spectra were measured at 90 K at electron beam energies ranging from 1 to 5 kV using an Oriel 260i instrument. Presented on Figure 5.2a are the CL spectra for NCD seeds, which gave a very weak signal. Figure 5.2b shows CL spectra for 1.8 μm unintentionally B-doped NCD on Si. The peaks at 1.84 eV, 4.87 eV, and 5.54 eV on Figure 5.2a could be matched by the peaks at 1.75 eV, 4.64 eV, and 5.44 eV, shown on Figure 5.2b. The peak at 1.84 eV could be attributed to isolated neutral vacancies or N vacancy complexes [136]. Emission from the 4.87 eV range has not been accounted for in the literature. Peaks in the 5-5.5 eV range are due to bandgap emission. The shift in peak energy values in the 5 nm thick NCD seed layer could be attributed to quantum confinement.

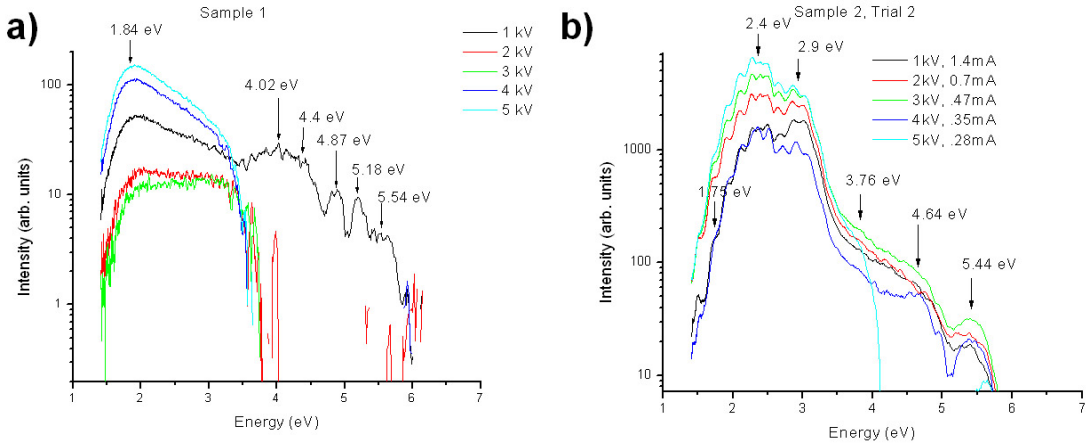

Figure 5.2: Cathodoluminescence spectra of (a) NCD seeds on Si and (b) 1.8 μm unintentionally B-doped NCD on Si. The NCD seeds gave a very weak signal.

5.2 Electrical Characterization of Doped and Undoped NCD Thin Films

Presented below are some capacitance-voltage measurements that illustrate some key aspects of NCD films. Two samples incorporating NCD films were fabricated. Their structures are presented in Fig. 5.3. The NCD films were 0.35 μm thick, but one sample had p^+ NCD film deposited on 50 nm of SiO_2 (sample A) and the other sample had undoped NCD from a B-free CVD reactor deposited directly onto the n-type Si substrate (sample B). As the NCD film on sample A was p^+ doped, it acted as a metal and therefore the structure was equivalent to an MOS capacitor with SiO_2 dielectric. Sample B was then equivalent to a metal-diamond-semiconductor capacitor. The Al layers on the front and back sides were 300 nm thick, deposited using e-beam evaporation, with no post-annealing performed. The top-side Al contact served as an etch mask for the NCD mesas, etched using a 200 W RIE process in O_2 plasma. Capacitance-voltage measurements were performed from the top-side to the back-side contact using a HP4275B LCR meter.

Fig. 5.4a shows the high-frequency (300 kHz) capacitance-voltage characteristics of the two samples. The flatband voltage V_{FB} was approximated as the voltage at which the capacitance is measured to be 80 % of the accumulation capacitance C_{OX}. V_{FB} of sample A was -0.7 V, which was in excellent agreement with MOS theory, and V_{FB} of sample B was -10 V, which indicated significant positive charge in the diamond layer. Carrier concentration analysis of the C-V data was performed and the results are shown in Fig. 5.4b. Using this analysis, the thickness of the NCD

film in sample B was confirmed.

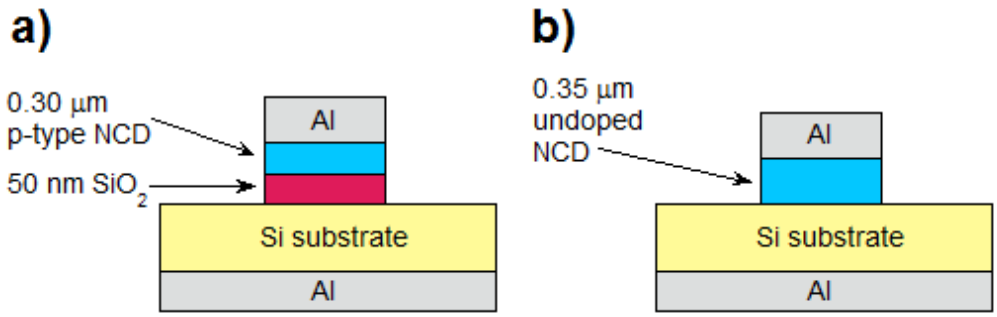

Figure 5.3: Samples structures of a) doped NCD on SiO_2 and b) undoped NCD on Si substrates.

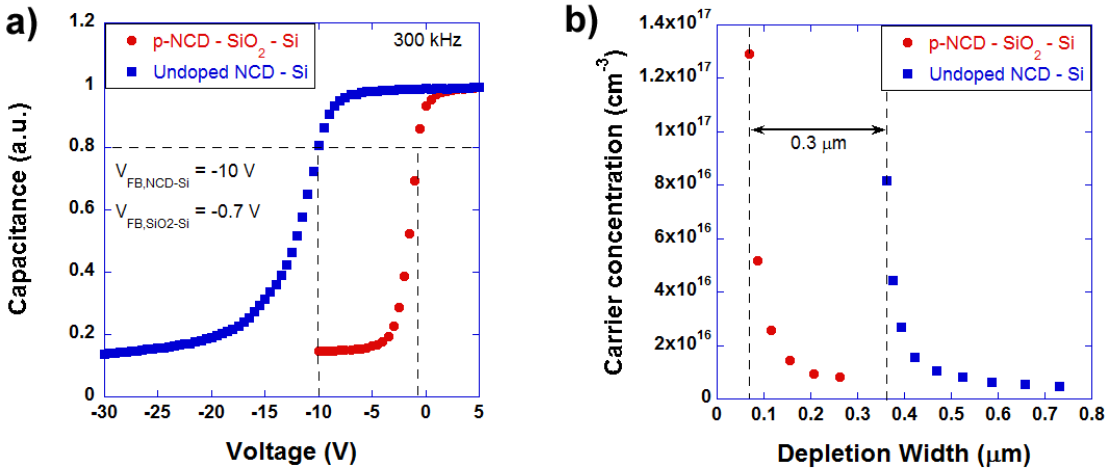

Figure 5.4: Capacitance-voltage characteristics of the samples from Fig. 5.3: the undoped NCD-Si interface as compared to the SiO_2-Si interface.

It would be curious at this point to compare the carrier concentration from CVD diamond grown on Si (Fig. 5.4b) to that of CVD diamond grown on single crystal diamond substrates. The diamond samples, courtesy of Dr. Jon Shaw at

NRL, had a 20 μm thick CVD diamond layer grown directly on square diamond substrates (about 5 mm wide). The CVD diamond was either doped p-type or non-intentionally doped. The C-V measurements were performed from the Cr top-side contact to the back-side substrate contact at 30 kHz to minimize series resistance effects. The carrier concentration profiles are shown in Fig. 5.8. The higher doped diamond layer (sample B) exhibited an interesting property: towards the surface, the carrier concentration decreased from about 1.2x10^{16} cm^{-3} to approximately 9.6x10^{15} cm^{-3}. This drop in free carrier concentration was due to the negative electron affinity of diamond (χ=-1.2 eV for ideal diamond), where surface electrons can escape to the vacuum level [105].

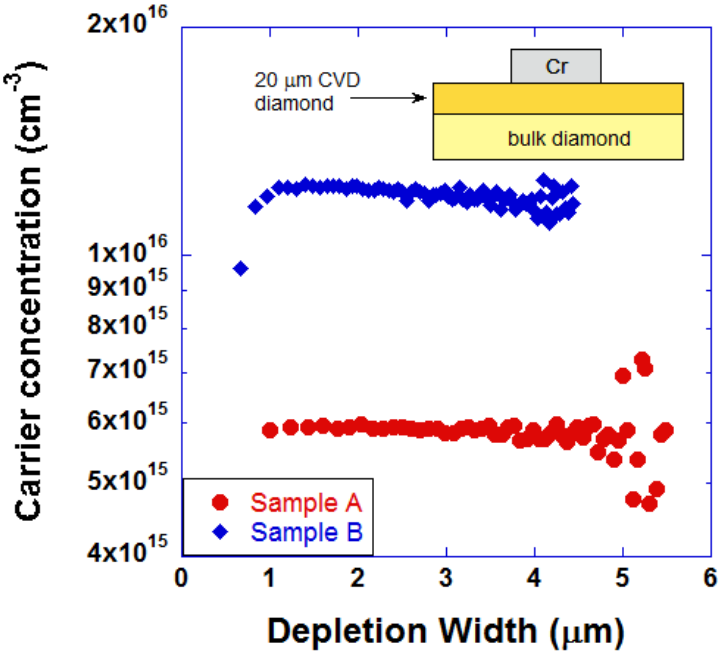

Figure 5.5: Carrier concentration profile of undoped and N-doped CVD diamond.

Providing an electrical contact to diamond depends on several factors. Apart from the diamond type (single crystal, polycrystalline, nanocrystalline), whose degree of sp^3 bonding determines the amount of defect-assisted conduction, the combination of factors that determines metal-diamond conductivity include diamond surface termination, doping (including ion implantation [137]), annealing conditions, and choice of metal. While the choice of metal can determine the work function difference, both Ohmic and Schottky contacts have been reported in the literature, typically using Ni, Ti, Au, or Al-based contacts. Figures 5.6 and 5.7 show rectifying contact behavior from high-pressure high-temperature (HPHT) grown CVD diamond.

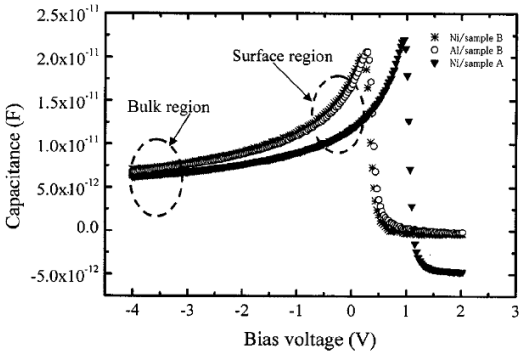

Figure 5.6: Capacitance-voltage curves of Ni and Al-based Schottky contacts to B-doped HPHT grown diamond [15].

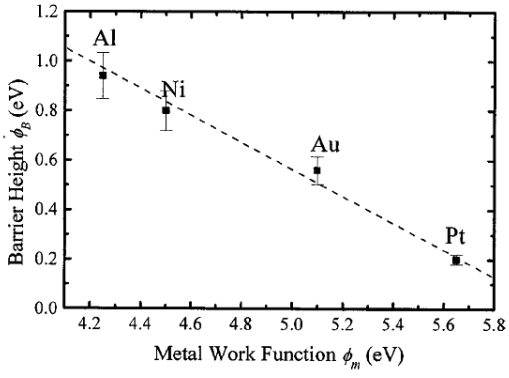

Figure 5.7: Schottky barrier height as a function of metal work function for Al, Ni, Au, and Pt based Schottky contacts to HPHT grown diamond [15].

It has been reported by Zhu et al. that the emission from diamond-based contacts increases as the defect density increases (Fig. 5.8. However, Sumant et al.

report a greater than 99 % sp^3 bonding for NCD films prepared using the modified NNP process [134]. Additional factors that could influence film conductivity include Carbon-related defects at the diamond interfaces. On the substrate side, in the case of Si, a very thin SiC layer could form during nucleation. On the metal-diamond interface, deposition of Ti has been reported to lead to the formation of TiC, which assists tunneling at the contact interface [138].

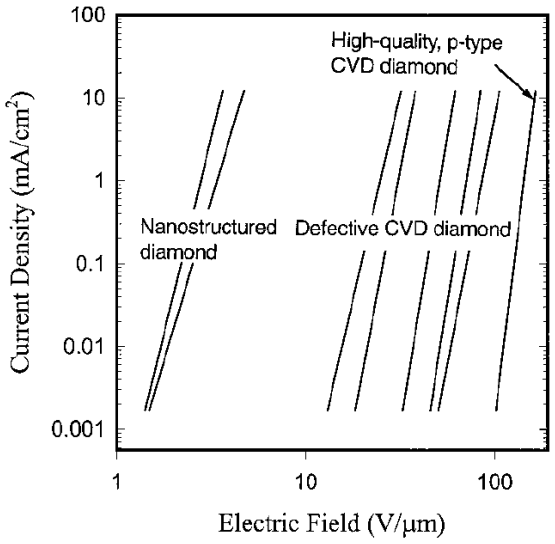

Figure 5.8: Current density vs. applied electric field for different types of diamond [16].

Looi et al. have reported conversion of rectifying Ti/Al contacts to H-terminated diamond to Ohmic by performing a 600 ℃anneal and surface rehydrogenation [139]. While they correctly point out that a contact could be erroneously reported as Ohmic when in fact a barrier height can be extracted from the curvature of the I-V characteristic, in the next section we present Ti/Al Ohmic contacts to non-intentionally doped H-terminated nanocrystalline diamond.

5.3 Comparative Study of Ohmic Contact Metallizations to NCD Thin Films

Four 4-inch Si wafers were coated with 100 nm plasma-enhanced CVD SiO_2. The wafers were initially cleaned in 4:1 H_2SO_4:H_2O_2 (piranha clean) for 10 min., followed by 10 min. in 1:1:5 NH_4OH:H_2O_2:H_2O (SC-1 clean), and finally immersed in 37 % HF for 1 min. They were then exposed to a nanodiamond-ethanol suspension solution to provide a seeded surface for diamond growth. 0.55 μm thick NCD films were grown in 0.3 % methane in hydrogen atmosphere (900 sccm total flow) at approximately 750 ℃ in a microwave plasma CVD system. A solution of 0.1 % diborane (B_2H_6) in hydrogen was introduced in the growth at flow rates ranging between 0 and 6 sccm. The resulting hole sheet density for the samples ranged between 10^5 and 10^{16} cm^{-2}, respectively.

Each wafer was diced into quarters, and each quarter was metallized by e-beam evaporation with Al, Ti/Al, Ti/Au, or Ni/Au. When present, the Ti or Ni contact metal layers were 20 nm thick, and the Al or Au overlay metal layers were 200 nm thick. The resulting 16 different quarters were further diced into eight samples each, for a total of 128 samples. Eight different annealing conditions were carried out on a sample from each quarter:

- 15 minute N_2 contact anneals in 1) 400 ℃, 2) 600 ℃, and 3) 900 ℃.
- 60 min., 400 ℃ in 4) N_2, 5) air (N_2/O_2), 6) O_2, and 7) forming gas (N_2/H_2).
- 60 minute 600 ℃ anneal in O_2.

Table 5.2: Sheet and specific contact resistivity to NCD as a function of NCD doping prior to annealing.

R_{SH} (Ω/sq.	0.1 % B_2H_6 in H_2 flow rate (sccm)			
	0	2	4	6
Al	6.17E+11	79194	2302.80	522.50
Ti/Al	4.07E+11	56238	1571.42	403.56
Ti/Au	3.28E+11	54840	1464.94	379.32
Ni/Au	4.21E+11	46446	1534.82	388.40

R_C (Ω-cm^2)	0.1 % B_2H_6 in H_2 flow rate (sccm)			
	0	2	4	6
Al	6.01E+5	8.83E-4	1.46E-6	4.08E-07
Ti/Al	3.75E+5	3.54E-3	6.71E-7	6.73E-06
Ti/Au	3.69E+5	4.06E-6	1.19E-4	1.10E-05
Ni/Au	2.32E+5	3.59E-4	2.71E-5	1.36E-05

Sheet resistance R_{SH}, specific contact resistivity R_C, sheet density, and mobility were measured before and after annealing using a transfer length method (TLM) pattern and a Hall probe. Table 5.2 summarizes the R_{SH} and R_C for the samples prior to annealing.

The sheet resistance decreased as the samples became more doped. The work functions of Ti, Al, and Ni are 4.33 eV, 4.28 eV, and 5.15 eV, respectively. The band gap of single crystal diamond is 5.5 eV, with electron affinity of –1.2 eV for hydrogen terminated diamond. Therefore, contacts with Ti and Al metal base provided an almost precise line-up of the Fermi levels at zero bias, and therefore a good natural Ohmic contact. This is evidenced in Table 5.2 by the low contact resistivity for Al and Ti/Al contacts at 4 and 6 sccm. The decrease of contact resistivity with doping suggested that thermionic emission dominated at low doping, whereas tunneling was

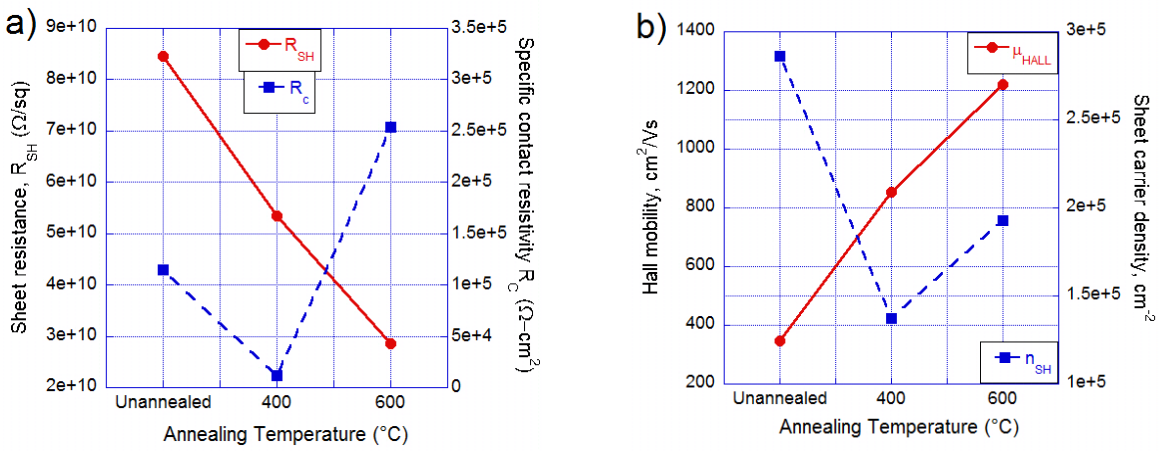

Figure 5.9: Effect of 15 min. N_2 contact anneal on the R_{SH},R_C, μ_{HALL}, and n_{SH} of non-intentionally doped NCD with a Ni/Au contact.

prevalent in samples doped with diborane flow higher than 4 sccm.

The effect of annealing the undoped films is presented on Figure 5.9. The choice of metals influenced the change in R_{SH} very slightly, with the exception of Al, which proved to be thermally unstable and degraded the sheet resistances of the undoped films. Here we present measurements using Ni/Au contacts, which had higher unannealed specific contact resistivity than Al-based contacts but yielded excellent Hall mobility for both the 400 ℃ and 600 ℃ anneals. Even though there was no intentional B doping in these films, a decrease in sheet resistance and increase in mobility indicated that H-passivated B near the surface may have been activated [140].

Figure 5.10 illustrates the effect of the different annealing atmosphere conditions on the non-intentionally doped NCD samples with Ni/Au contacts. The samples were annealed at 400 ℃ for 60 minutes. The highest reduction in sheet

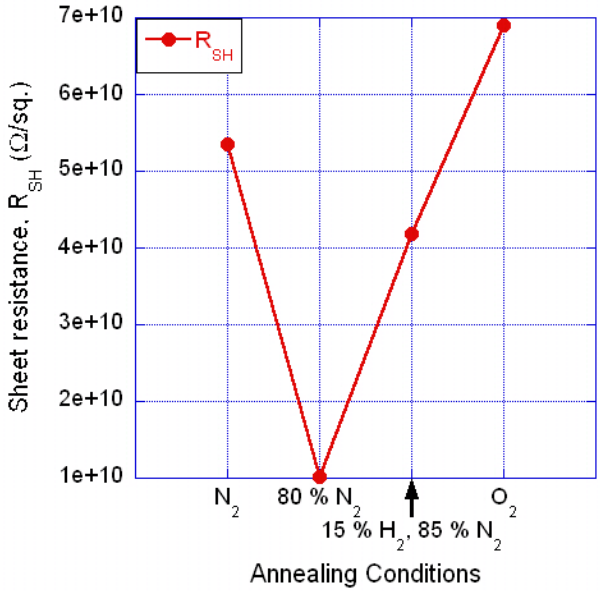

Figure 5.10: Effect of 400 ℃ film anneals in N_2, air, forming gas, and O_2 on the sheet resistance of non-intentionally doped NCD (0 sccm B_2H_6) with a Ni/Au contact.

resistance was achieved in air atmosphere (80 % N_2), whereas annealing in pure O_2 slightly etched the NCD and this degraded the sheet resistance.

The effect of annealing on the doped samples was minimal. Two notable exceptions were the 600 ℃, 1 hour anneal in O_2, which had severely etched the diamond film, and the 900 ℃ 15 min. anneal in N_2, which increased the specific contact resistivity in the doped films by several orders of magnitude. Otherwise, R_{SH} on the doped samples remained within 5 % of the value measured before annealing.

5.4 Chapter Summary

In this chapter, the sheet resistance, contact resistance, and mobility of p-type NCD thin films were investigated using the TLM and Hall methods. Increasing

the diborane flow rate from 0 to 6 sccm decreased the sheet resistance over nine orders of magnitude. Al-based Ohmic contacts resulted in lower contact resistivity for higher-doped NCD films than Au-based contacts. Contact annealing in N_2 for 15 minutes up to 600 ℃ lowered the R_{SH} and increased Hall the mobility of undoped NCD films.

Chapter 6

Nanocrystalline Diamond as an Electral and Optical Contact to 4H-SiC

This chapter presents research into the electrical properties NCD/SiC heterojunctions. Both doped and undoped layers of NCD are deposited on n- and p-type 4H-SiC epitaxially grown layers. We suggest a trap-assisted tunneling conduction mechanism.

Previously, cathodoluminescence data of deep levels in NCD was given in Chapter 5. Here, in Section 6.2, we focus on deep level studies of 4H-SiC devices using thermally stimulated current (TSC) methods. TSC spectra from p-type MOS capacitors and n-channel MOSFETs indicated the presence of oxide traps with peak emission around 55 K. An additional peak near 80 K was observed due to acceptor activation and hole traps near the interface. The physical location of the traps in the devices was deduced using a localized electric field approach, which is explained in detail in Section 6.3.

6.1 UV-Semi-Transparent Nanocrystalline Diamond Films as a Type-II Heterojunction to 4H-SiC

Nanocrystalline diamond (NCD) thin films are of interest due to their large bandgap and excellent thermal properties, which make them attractive for power

device applications [134, 141, 104, 142]. The thermal conductivity of NCD films with a nucleation density larger than 10^{12} cm^{-2} has been shown to reach 12.7 W/cm-K for a 3.5 μm thick film. [133] While the UV semi-transparency of NCD films has been previously reported on other substrates [135], here we show that both doped and undoped NCD films can also be used as an electrical contact for both n- and p-type 4H-SiC, allowing for the simultaneous measurement of both the optical and electrical characteristics of wide-bandgap semiconductor devices.

Three sample structures were used, with the NCD grown via microwave plasma-enhanced chemical vapor deposition. The sample structures were: (1) 0.5 μm thick B-doped p^+ NCD on a 5μm n^- 4H-SiC epitaxial layer, (2) a similar NCD film on a 10 μm p^- 4H-SiC epilayer and (3) an unintentionally-doped NCD film on a 10 μm n^- 4H-SiC epilayer. All SiC epilayers were grown on 8° off $< 0001 >$ towards $< 11\bar{2}0 >$ 4H-SiC n^+ ($n>1x10^{18}$ cm^{-3}) substrates. The n- and p-type SiC epilayers had carrier concentrations of approximately $2x10^{16}$ cm^{-3}. Details of the SiC epitaxial growth have been reported elsewhere [143].

The SiC samples were initially cleaned in 4:1 H_2SO_4:H_2O_2 (piranha clean) for 10 min., followed by 10 min in 1:1:5 NH_4OH:H_2O_2:H_2O (SC-1 clean), and finally immersed in 37 % HF for 1 min. They were then exposed to a nanodiamond-ethanol suspension solution to provide a seeded surface for diamond growth [127, 128]. Film growth was initiated in a dilute methane atmosphere at 750 ℃in a microwave plasma CVD system. Diborane introduced in the growth was sufficient to yield approximately $7x10^{19}$ atoms/cm^2, which was expected to give a hole concentration of between 1–$10x10^{18}$ cm^{-3}. The undoped NCD film was grown in a separate chamber

that was not contaminated with Boron and therefore was capable of producing extremely pure films with very high resistivity (>10^{10} ohm-cm) [144].

Three hundred nm thick Al contacts were deposited onto the front side of the samples. For the I-V and C-V measurements the contacts were circular with 350 μm diameter. For the EL and OBIC measurements the contacts were a rectangular grid with open spaces to allow for light collection, as shown on Figure 6.2. A blanket Al film was also deposited on the back side of all samples to lower the contact resistance. Device isolation was achieved by an O_2-RIE etch using the Al layer as a mask. Two-point I-V measurements were performed using an HP4145B semiconductor parameter analyzer using the probe station chuck as a back side contact. The C-V measurements were performed using an HP4275A LCR meter. A detailed description of the OBIC and the EL setups can be found in the literature [110].

All three samples exhibited a highly Schottky-like rectifying behavior (Figure 6.1), suggesting a metallic nature for the p^+ NCD film. In the case of p^+ NCD / n^- SiC a forward-bias exponential increase in the current was observed over 8 orders of magnitude. The ideality factor ranged between n=1.17 at 30 ℃ and 1.07 at 210 ℃. In contrast, the p^+ NCD on p^- SiC fell between n=1.92 at 30 ℃ and 1.75 at 210 ℃. The ideality factor of the undoped NCD film on n^- SiC was found to be similar to that of the p^+NCD on n^- SiC, with values between n=1.14 at 30 ℃ and 0.93 at 210 ℃. The relative stability of the I-V characteristics with temperature and the negligible reverse leakage current levels (approximately 10^{-8} A/cm^2 and up to 3x10^{-7} A/cm^2 at -20V for p^+NCD on n^- SiC) demonstrate that NCD is a versatile high-temperature contact to 4H-SiC.

Due to non-uniformities in the nanodiamond seed layer, the size of the electrically active area under the Al contacts may not be known exactly. For this reason, and because the Richardson's constant A** for this heterojunction is currently unknown, a standard current-temperature barrier height measurement method was employed [102, 145]. In general, Schottky barrier height is defined as the difference between the metal work function ϕ_M and the semiconductor electron affinity χ [102]. For the p^+ NCD / n^- SiC sample, the corresponding barrier height was the energy difference between the NCD Fermi level and the SiC conduction band. An exponential fit was performed on the measured current to obtain a value for the current I_o at zero bias (V_F= 0 V). The barrier height ϕ_B was calculated from the Richardson plot (Figure 6.1a inset) via the slope of the Arrhenius expression $\ln(I_o/T^2) = \ln(A_e A^{**}) - q(\phi_B - V_F)/kT$, where A_e is the size of the electrically active area and k is Boltzmann's constant. The nonlinear nature of some curves on the Richardson plot suggested a temperature dependent barrier height [102]. However, from a linear fit of the data on the Figure 6.1a inset, the extracted values of ϕ_B for p^+ NCD / n^- SiC, p^+ NCD / p^- SiC and undoped NCD / n^- SiC were 0.84 eV, 0.74 eV, and 0.47 eV, respectively.

Independent capacitance-voltage measurements of the barrier heights are shown in Figure 6.1b. In this method, the barrier height is related to the x-axis intercept V_i by $\phi_B = -V_i + V_0 + kT/q$, where V_0 is the bulk potential of the SiC epilayer based on the effective density of states ($3.25 \times 10^{15} \times T^{3/2}$ cm^{-3}) rather than the intrinsic carrier concentration [1, 102]. Using this approach, the barrier heights were found to be 0.82 eV, 2.35 eV and 3.8 eV for the p^+ NCD / n^- SiC, p^+ NCD /

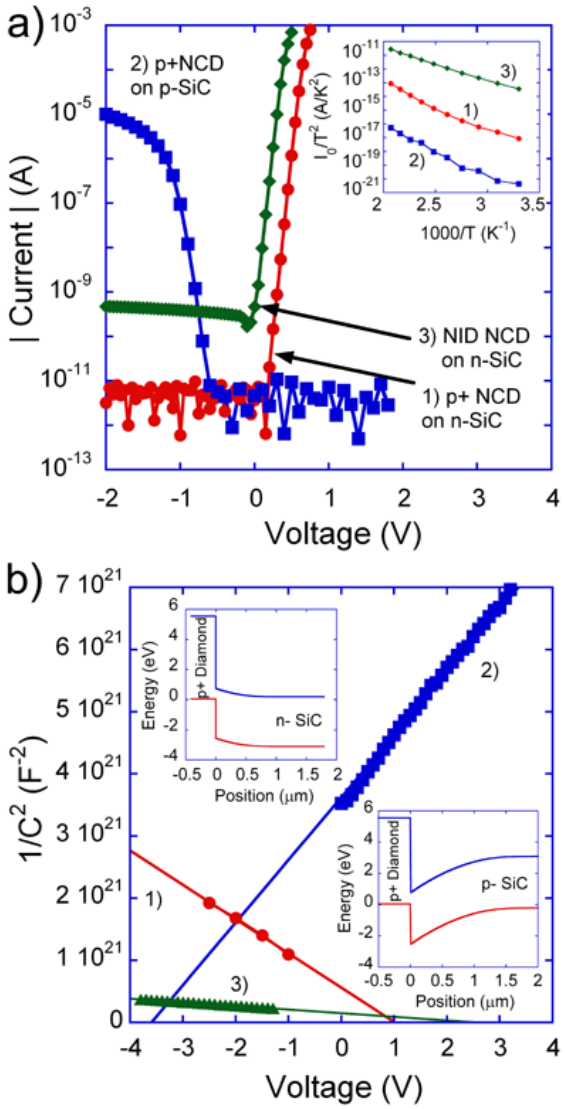

Figure 6.1: a) Current-voltage characteristics of the three samples. The inset shows the Richardson plot from the current-temperature method used to determine the barrier heights: 1) $\phi_B = 0.85$ eV, 2) $\phi_B = 0.74$ eV, 3) $\phi_B = 0.48$ eV. b) Capacitance-voltage data used to determine the barrier height of each heterojunction: 1) $\phi_B = 0.82$ eV, 2) $\phi_B = 2.35$ eV, 3) $\phi_B = 3.8$ eV. The two insets show the ideal energy-band diagrams of diamond on n- and p-SiC.

p^- SiC and undoped NCD / n^- SiC, respectively. The discrepancies between the barrier heights extracted using the I-V and C-V methods are discussed later in this letter.

Ideal energy-band diagrams were calculated using the Silvaco© device simulator for p^+ diamond on n^- and p^- SiC and are inset on Figure 6.1b. For simulation purposes, H-terminated diamond electron affinity of χ=-1.2 eV and bandgap of E_G=5.5 eV were used [105]. A type-II heterojunction behavior was determined, where $\chi_{NCD} < \chi_{SiC}$ and $\chi_{NCD} + E_{G,NCD} < \chi_{4H-SiC} + E_{G,4H-SiC}$, with χ_{4H-SiC} = 3.5 eV and $E_{G,4H-SiC}$ = 3.2 eV [146]. From these simulations, a possible conduction path can be identified between the conduction band of the SiC and the B-impurity band of the NCD. Another conduction mechanism could be trap-assisted-tunneling at the NCD-SiC interface, due to the close proximity of the bands at the NCD/SiC interface. A trap-assisted-tunneling model was proposed by Danielsson *et al.* for the case of the GaN-SiC heterojunction [147]. Here, the exact doping and quality of the seed layer from which the NCD film was nucleated is currently unknown and may itself act as a metal-like conductor. It is known, however, that the significant concentration of nitrogen in the nanodiamond seed found to reside 1.7 eV to 4 eV below the conduction band would be too deep to sufficiently increase the film conductivity [148, 149]. Finally, spatially indirect generation processes in type-II heterojunctions can occur due to wave function overlap between electrons in the conduction band and holes in the valence band without the assistance of traps at the interface. Such processes have been experimentally observed via photoluminescence [150] and modeled using density-gradient theory [151].

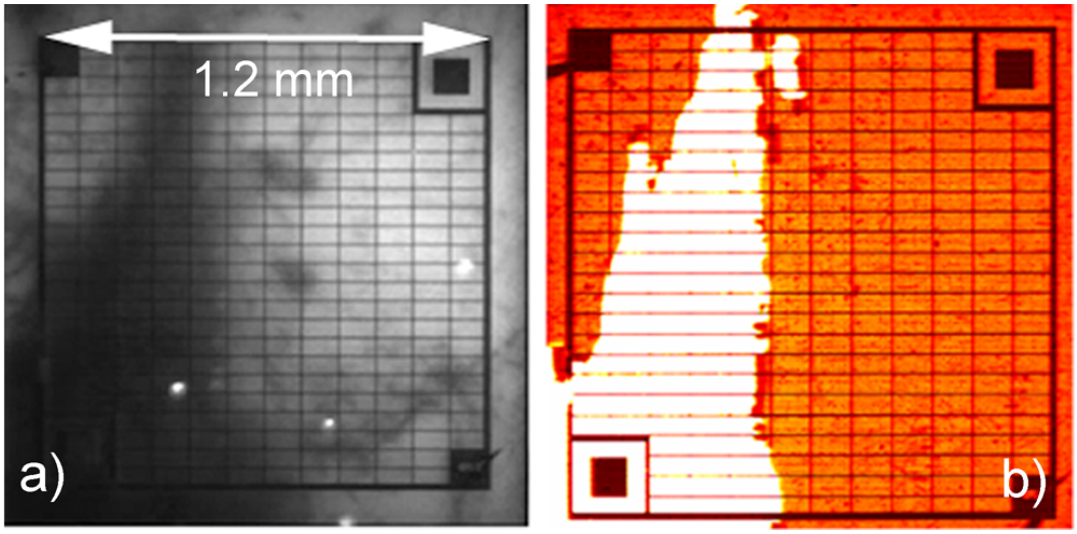

Figure 6.2: EL (a) and OBIC (b) images of 4H-SiC with NCD blanket film. UV-semi-transparency of NCD allowed for the simultaneous biasing and imaging of the underlying 4H-SiC

The presence of defects at the NCD-SiC interface helps explain the mismatch between the I-V and C-V extracted barrier heights. The barrier height extracted using I-V data was from a forward-biased junction, where both trap-assisted tunneling and band-to-band recombination may have taken place. This barrier height would represent the lower-barrier regions on the device where preferential injection took place due to the presence of interface traps. On the other hand, the C-V data was measured in the depletion region, which corresponded to the reverse bias of the I-V data. As such, C-V analysis did not account for trapping effects because the carriers were repelled from the interface, and the barrier height calculated was an average value over the entire device area. Defects at the interface can act either as recombination centers or intermediate states for trap-assisted tunneling currents,

and both mechanisms raise n and lower the I-V extracted ϕ_B [102]. This was the case for both p^+ NCD / p^- SiC and undoped NCD / n^- SiC samples (1.61 eV and 3.33 eV mismatch, respectively). The larger mismatch for the undoped NCD sample could be partially attributed to additional barrier lowering induced by the hole accumulation layer (density of about 10^{13} cm^{-3}) at the surface of undoped H-terminated diamond [152]. However, such charge density was not enough to account for the 1.72 eV difference in barrier height between the two samples. Further experiments and simulations are underway to help explain the precise conduction mechanisms taking place in the NCD-SiC heterojunction.

OBIC and EL images, presented on Figure 6.2a and 6.2b, revealed two important applications for NCD films. We used the NCD film as a UV-semi-transparent contact to the underlying epitaxial layer to perform optical measurements, and as a Schottky electrical contact to provide a means of forward-biasing these junctions while still allowing light to be externally collected. In the EL image, the bright spots exhibited a yellow-blue luminescence, and therefore could be tentatively identified as threading edge dislocations [153]. A dark (bright) triangular-shaped defect dominates the EL (OBIC) images and was found to correspond to a region of a 6H-SiC polytype inclusion.

The extremely low turn on voltage and high on/off current ratio of the NCD/SiC heterojunctions studied here means that these devices have potential application as low voltage sensors (e.g., energy harvesters, rectennas). An important figure of merit for such devices is their sensitivity γ, a.k.a curvature coefficient, defined as the ratio of the second derivative to the first derivative of the current-voltage char-

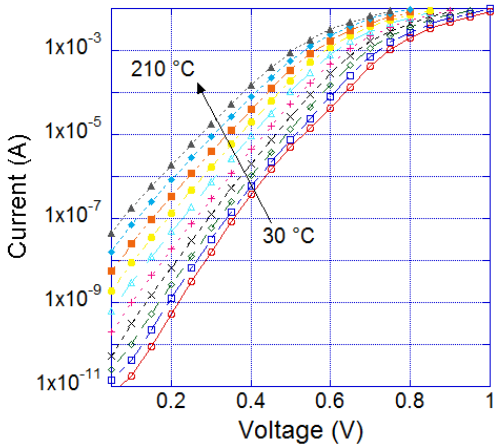

Figure 6.3: Temperature-dependent current-voltage characteristics of the $p^+ - NCD/n^- - SiC$ diode.

acteristic [145]. Figure 6.3 and Eqn. 6.1 were used to extract the sensitivity curves in Fig. 6.4.

$$\gamma = \frac{d^2I/dV^2}{dI/dV} \tag{6.1}$$

Figures 6.4a and 6.5a present the sensitivity temperature dependence for doped and undoped NCD/SiC heterojunction diodes. A value of about 105 V^{-1} at zero bias and room temperature for the $p^+ - NCD/n^- - SiC$ diode indicates that tunneling dominates the conduction mechanism, as classic p-n and Schottky diodes have a maximum sensitivity of 1/kT (about 38) V^{-1}. Sensitivity over 100 exceeds that of Si-based backward diodes [154], Ge tunneling and backward diodes [155], Al/GaAs low-barrier Schottky diodes [156], and MIM (metal-insulator-metal) diodes [157, 158].

The sensitivity for the NCD/p-SiC diode, exhibiting backward diode behavior in Fig. 6.1a, was less than 10 (not plotted here).

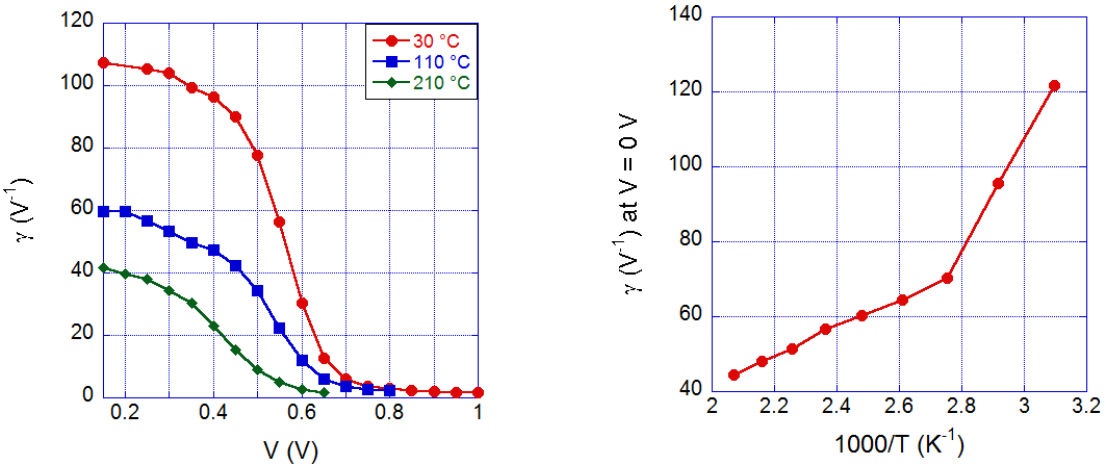

Figure 6.4: Curvature coefficient vs bias and temperature for p+ NCD / n- SiC heterojunction.

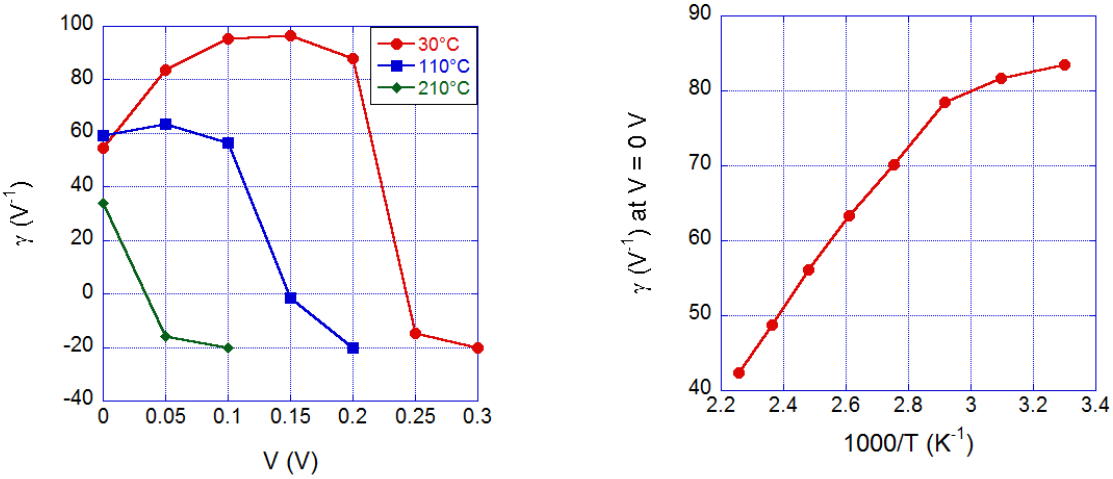

Figure 6.5: Curvature coefficient vs bias and temperature for non-intentionally doped NCD/n^{-}-SiC heterojunction.

Figures 6.4b and 6.5b show the temperature dependence of the sensitivity at zero bias, extracted from the previously presented plots. The wide variation with temperature is in contrast with the theory of tunneling diode conduction, where γ has been consistently shown to be very weakly dependent on temperature. This raises the question of the type of tunneling diode that the NCD/SiC heterojunction constitutes. Traditionally, a tunneling diode consists of degenerately doped p and n regions in order to push the Fermi levels into the allowed bands. However, none of our samples were degenerately doped, and one sample even had undoped NCD. A backward diode does not necessarily need degenerate doping, and we did previously observe backward diode behavior in Fig. 6.1a. However, the sensitivity of backward diodes depends very weakly on temperature.

The I-V characteristics, as well as the strong temperature dependence of the sensitivity in our samples, is more consistent with the behavior of an MIS diode with a very thin insulator layer (less than 3 nm thick). In this case, the role of the insulator is likely played by the nanodiamond seed layer. To verify this hypothesis, the dependence of the current on the nanodiamond seed film thickness, as well as the diamond and SiC layer doping densities, needs to be quantified in the future.

6.2 Bulk Trap Characterization of 4H-SiC Devices Using Thermally Stimulated Current

Techniques of defect analysis by measuring luminescence or electrical current due to the thermal generation of electron-hole pairs during ionization have been well known to the semiconductor research community. Nicholas and Woods characterized electron traps in CdS by measuring its luminescence as a function of temperature [159]. Buehler and Phillips measured the TSC spectra of intentionally introduced Au acceptors in the base region of bipolar devices in their studies of lifetime suppression in transistor-transistor logic (TTL) circuits [160]. Extensive work has been performed by Fleetwood *et al.* on nitrided oxides [161] and irradiated MOS devices [162, 163]. The experimental results from their work advanced the theoretical understanding of thermally activated processes. [164–167]

A contributing factor to the low field effect mobility of SiC MOSFETs has been suggested to be traps near the SiC/SiO_2 interface. However, the physical nature or location of these interface traps is still under investigation in the SiC community. Energetically spread throughout the band gap of the material, carrier traps behave as additional acceptors near the conduction band or donors near the valence band. When located near the SiO_2/SiC interface, their influence on the transport properties of the device can be detrimental [168].

Previous reports of TSC measurements on SiC have focused on MOS capacitors fabricated on n- and p-type 4H- and 6H- epitaxial layers [169–172]. Studies of p-type 6H-SiC MOS capacitors by Lysenko [169] and Ólafsson [170] showed two main

peaks in the TSC spectra, located at approximately 50 K and 70 K. The origin of the former peak was attributed to interface states, whereas the latter was concluded to be due to Al acceptors (E_A = 160 to 230 meV) [173–175]. On n-type 4H-SiC, Rudenko *et al.* had observed TSC peaks near 40 K, 90 K, and 150 K [171, 172]. The 40 K peak was attributed to N donor ionization, and the other two peaks were due to the presence of interface states near the conduction band. In addition, Fang *et al.* have performed TSC characterization of 4H-SiC substrates, identifying Al, B, and V defect levels at 0.22 eV, 0.28 eV, and 0.91 eV, respectively [176].

To the authors' knowledge, TSC experiments on MOS transistors have not been previously reported in the literature. Here, we characterize the TSC spectra of MOS capacitors, and then present a method of separation of the observed traps. We do so by using transistor samples, where separate electric fields could be localized to the oxide and the bulk of the device. Furthermore, we present a method of separating the contribution of different emission mechanisms to peaks at the same temperature using gamma ray irradiation. Both methods are described in the experimental results section.

6.2.1 Experimental Details

In this work, we used 5 μm thick epitaxial p-type (Al doped, N_A=1x10^{16} cm^{-3}) 4H-SiC MOSCAP and p-channel lateral LDMOSFET samples with circular metal contacts, provided by Cree, Inc. The thickness of the thermally grown SiO_2 was 500 Å, NO-annealed using standard post-oxidation techniques. Details about device

fabrication can be found elsewhere in the literature [177].

Specifying the temperature for entering the carrier freeze-out regime was essential for interpreting TSC spectra. In this work, we did so by observing the decrease of the accumulation capacitance at cryogenic temperatures. The capacitance-voltage (C-V) measurements were performed using a Keithley 590 capacitance meter. Figure 6.6 shows the temperature dependent C-V behavior of a 4H-SiC MOS capacitor swept at 100 kHz from accumulation to depletion. At temperatures lower than 160 K, the device entered the freeze-out regime and the hole accumulation layer density was very low. For comparison, shallow N donors with activation energy of around 50 meV in n-type SiC samples ionized around 50 K [171].

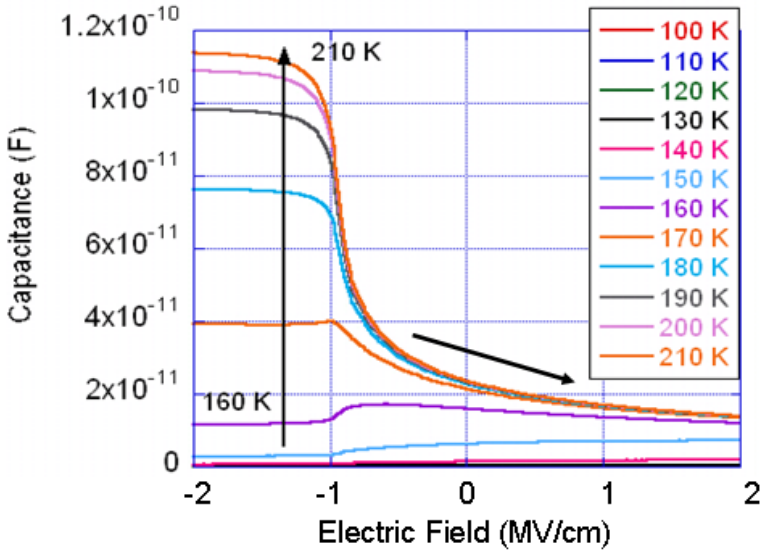

Figure 6.6: High frequency (100 kHz) C-V characteristics as a function of temperature of an epitaxial p-type 4H-SiC MOS capacitor.

A similar C-V measurement was performed on a capacitor-connected MOS transistor with source, drain, and body connected together. The resulting curves

are shown in Fig. 6.7. The accumulation layer behavior is identical to the one observed in Fig. 6.6. However, due to the presence of a source and drain in the device, an inversion layer was maintained at all temperatures, including below the lowest temperature shown in Fig. 6.7, down to 16 K.

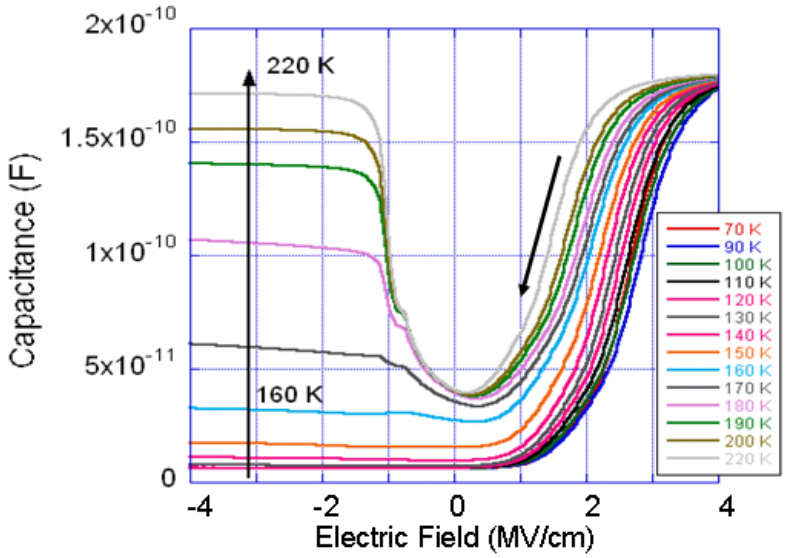

Figure 6.7: High frequency (100 kHz) C-V-T characteristics of the n-channel 4H-SiC MOSFET device. Source, drain, and body of the FET were connected together.

The samples were mounted on an insulating AlN pad, wirebonded to a chip carrier, and placed in a flow through Janus dewar. The TSC spectra were measured using Keithley 617 and 6517 electrometers. No curve smoothing algorithms have been applied to the TSC spectra reported in this work. Each cycle of cooling and warmin completed in approximately two hours, with custom software automating the tasks of a Lakeshore 91-C temperature controller and a liquid He tank pressure control setup.

Samples were cooled down to 250 K, at which point a gate bias was applied,

with either positive or negative polarity [171]. While maintaining the bias on the gate, the samples were cooled down to about 20 K, at which point the polarity of the gate bias was reversed and the heater inside the dewar was turned on. As the temperature increased back to 250 K, the current was recorded and any peaks observed were reported as TSC spectra.

Table 6.1 summarizes the conditions under which the TSC measurements were performed. The magnitude and the polarity of the gate field, approximated by $E = V_G/t_{OX}$, were varied during cooldown ($E_{cooldown}$) or warmup (E_{warmup}). As a result, the device would be either in accumulation or depletion/inversion during cooldown and the opposite condition during warmup. For the MOS transistors (source and drain tied together), additional variables were the body bias (V_{body}) and the source/body junction bias ($V_{S/B}$). The heating rate (β), though not specifically controlled, was consistent among all measurements. It was highest at cryogenic temperatures (0.19 K/s) and decreased as room temperature was approached (0.04 K/s at 160 K, the highest temperature at which a TSC peak was observed). This variation was taken into account when calculating trap densities.

6.2.2 Results and Discussion

6.2.2.1 Spatial Separation of Carrier Traps (localized electric field method)

Two methods for TSC carrier trap characterization are presented in this work. The first method, described in this section, allowed us to obtain information about

Table 6.1: Summary of device setup and TSC measurement conditions.

Device	**Fig.**	**Details**	**Cooldown**	**Warmup**
MOSCAP	6.6	Electrometer on gate	$E_{cooldown}$ = -2 MV/cm Accumulation	E_{warmup} = 1 to 5 MV/cm Depletion
MOSCAP	6.7	Electrometer on gate	$E_{cooldown}$ = -2 to -4.5 MV/cm Accumulation	E_{warmup} = 2 MV/cm Depletion
MOSFET	6.9	Electrometer on gate	$E_{cooldown}$ = -2 MV/cm Accumulation	E_{warmup} = 2 to 5 MV/cm Inversion
MOSFET	6.10	Electrometer on back side contact (body)	V_{body} = -10 to -25 V $E_{cooldown}$ = -4 MV/cm Accumulation	V_{body} = -10 to -25 V E_{warmup} = 2 MV/cm Inversion
MOSCAP	6.12a	Electrometer on gate; 100 krad γ-irradiation with 2 MV/cm gate field (depletion) prior to TSC	$E_{cooldown}$ = -1 to -4 MV/cm Accumulation	E_{warmup} = 2 MV/cm Depletion
MOSCAP	6.12b	Electrometer on gate; 100 krad γ-irradiation with -2 MV/cm gate field (accumulation) prior to TSC	$E_{cooldown}$ = -1 to -4 MV/cm Accumulation	E_{warmup} = 2 MV/cm Depletion
MOSFET	6.13	Gate and drain floating, electrometer on source-body junction	$V_{S/B}$ = 2.5 V Forward Bias	$V_{S/B}$ = -20 to -100 V Reverse Bias

the physical location of traps in the device by comparing the TSC spectra of an MOS capacitor and an FET from the same die. We first measured the TSC spectra of an MOS capacitor, biased in accumulation during cooldown and depletion during warmup. Two peaks were observed, near 55 K and 80 K, as presented in Fig. 6.8 and 6.9. During the warmup cycle, the gate field terminated on the back side metal contact due to the lack of an inversion layer at the SiO_2/SiC interface. As a result, TSC spectra obtained using this arrangement originated from traps located throughout the entire device.

Next, we measured an adjacent MOS transistor. Two electrometers were connected to the device, one to the gate and one to the back side body contact, as shown in Fig. 6.11. First, we held the body bias steady and varied the gate bias. During warmup, the inversion layer of the MOSFET acted as a gate field termination layer, thus isolating the emission of any resulting TSC to the area between the gate metal and the bottom of the inversion electron sheet. Figure 6.11 shows that only the 55 K peak was measured by the gate electrometer in the temperature range covered. Peaks similar to the ones shown in Fig. 6.12 were registered near 80 K by the body electrometer. Therefore, the 55 K peaks originated from traps localized within the gate electric field terminating on the inversion layer, and the 80 K peaks obtained from the capacitor measurements should originate from the SiC bulk or epilayer. To verify this hypothesis, the MOSFET was measured again, this time with constant gate bias and variable body bias. Figure 6.12 verified that only the 80 K peaks were registered by the body electrometer, whereas the gate electrometer only registered peaks at 55 K (identical to Fig. 6.11, not shown for brevity).

The following sections provide further insight into this technique, as well as some additional artifacts that could influence the results.

A. TSC Spectra of MOS Capacitors

To verify the validity of the local electric field approach described above, we considered the configuration where the capacitor was biased in accumulation during cooldown and inversion during warmup. By using a capacitor instead of a transistor, the formation of a gate field terminating inversion layer was avoided when the gate bias was switched from accumulation to depletion at 20 K. During warmup, the hole accumulation layer remained frozen out and the gate field terminated on the n^+ SiC substrate, rather than the oxide/epi interface. The resulting TSC spectra, shown in Fig. 6.8 and 6.9, exhibited two peaks of positive current near 55 K and 80 K. Since there were virtually no electrons present in the SiC epilayer ($n_{i,4H-SiC,80K}$ = 4.95x10^{-84} cm^{-3}) [1], the TSC must have been due to positive charge flowing away from the gate and into the substrate.

The density of traps, N_t, associated with the 55 K and 80 K peaks, were calculated by integrating the TSC spectra using Equation 6.2,

$$N_t = \frac{1}{\beta A q} \int_{T_1}^{T_0} I(T) dT \tag{6.2}$$

where A is the device area and q is the electron charge [178].

For the 55 K peak in Fig. 6.8, $N_{t,55K}$ = 1.35x10^{12} cm^{-2} at 4 MV/cm gate field, and similar values for the other fields. The trap density as a function of gate field for the 80 K peaks in Fig. 6.8 and 6.9 is presented in Fig. 6.10.

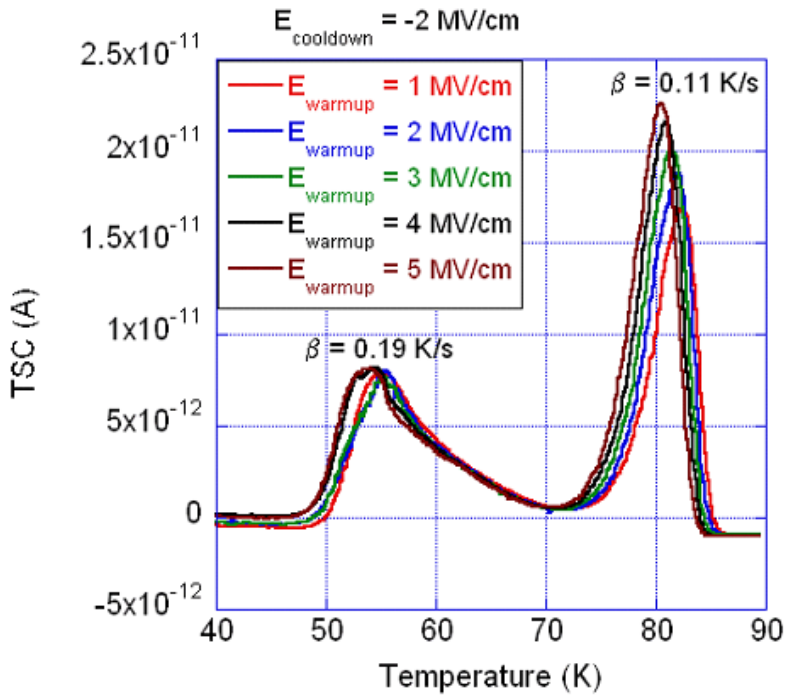

Figure 6.8: TSC spectra of a p-type epitaxial 4H-SiC MOSCAP biased in accumulation during cooldown ($E_{cooldown}$ = -2 MV/cm) and depletion during warmup.

The 5 MV/cm TSC peak in Fig. 6.8 (23 pA at 80.5 K) yielded trap density of $N_{t,80K}$ = 1.3 x 10^{16} cm^{-3} (3.25x10^{12} cm^{-2}) [1]. Even though this was very close to the p-type epilayer Al doping level of $N_A = 10^{16}$ cm^{-3}, it must be noted that that only a small fraction of the Al acceptors were electrically active at 80 K [179]. Neither peak of the TSC spectra in Fig. 6.8 exhibited a strong dependence on the depletion bias during warmup. One interesting observation was the shift of the 80 K peak

[1]When expressing $N_{t,80K}$ as a volume density, we used a value of 2.5 μm (half of the 5 μm SiC epilayer thickness) for the depletion width, since at cryogenic temperatures a depletion region did not exist. Using half the SiC epilayer thickness accounted for the average contribution to the measured current of carriers traversing the epitaxial region.

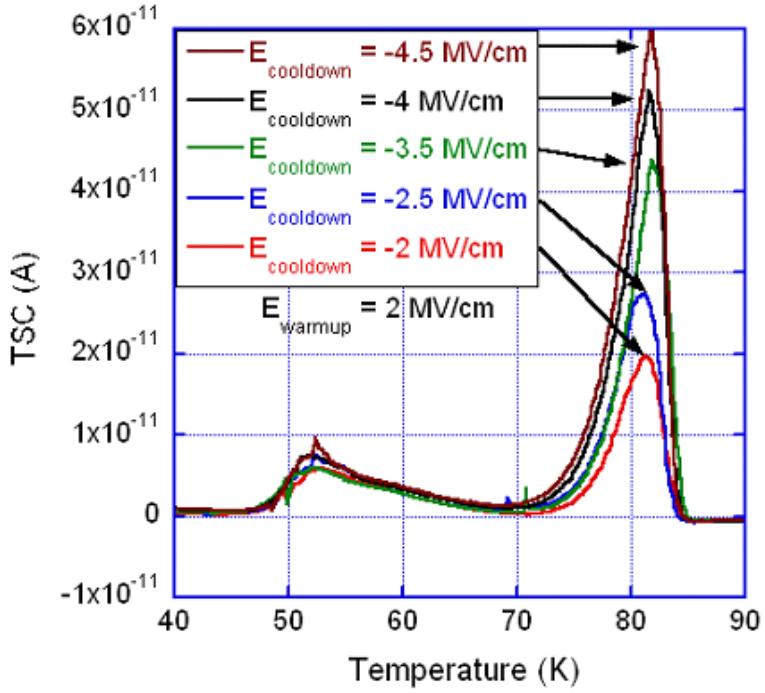

Figure 6.9: TSC spectra of a p-type epitaxial 4H-SiC MOSCAP biased in accumulation during cooldown and depletion during warmup with a constant warmup field E_{warmup} = 2 MV/cm.

temperatures (T_{max}) to lower values as the depletion bias increased. This shift is caused by the Poole-Frenkel effect, where the traps' energy level shifted towards the valence band as the gate field increased ($E\text{-}E_t \propto E_{GATE}^{1/2}$) [180].

In Figure 6.9, when the device was biased at different accumulation levels during cooldown, $N_{t,55K}$ remained almost constant (1.33x10^{12} cm^{-2}), whereas $N_{t,80K}$ depended strongly on the density of the accumulation layer. $N_{t,80K}$ at 4.5 MV/cm had increased to 3.36x10^{16} cm^{-3} (8.41x10^{12} cm^{-2}), which suggested an excess hole trap concentration of 5.6x10^{12} cm^{-2} near the SiO_2/SiC interface, where the hole accumulation layer was formed. The presence of hole traps near the valence band

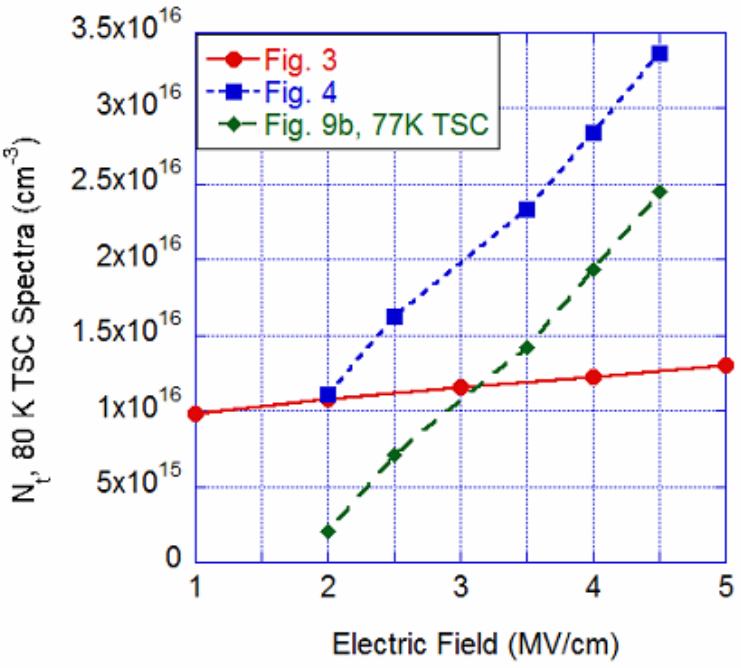

Figure 6.10: N_t as a function of gate field for the 80 K TSC spectra from Fig. 6.8 and 6.9, as well as the 77 K TSC spectra in Fig. 6.14b.

in bulk SiC has been previously observed by Danno *et al.*, who reported minimal influence of these traps on the carrier lifetime [181]. Rozen *et al.* have attributed the higher density of hole traps in NO-annealed oxides to the increased nitrogen incorporation at sites near the interface [182].

B. TSC Spectra of MOS Transistors

To determine the physical location of trap emission within the device, we performed a TSC measurement on an MOS transistor biased in accumulation during cooldown and inversion during warmup. To do so, we had to ensure that the applied gate bias was high enough to keep the device in inversion as the threshold voltage increased at cryogenic temperatures.

Several groups have previously explored the temperature dependence of the threshold voltage in 4H-SiC MOSFET devices at high temperatures [183–185]. Due to the dramatic decrease in effective carrier concentration in SiC over the measured temperature range, the sample exhibited V_{th} increase from about 0.73 V at room temperature to 7.4 V at 40 K, as extracted from the x-intercept of the I_D vs. V_{GS} curve at $V_{DS} = 0.1$ V. This change in V_{th} indicated a net *negative* charge of $3x10^{12}$ cm^{-2} present in the oxide. The field-effect mobility (μ_{FE}) decreased from 26.9 cm^2/Vs at room temperature to less than 5 cm^2/Vs below 100 K, as previously reported in the literature [186].

As shown by the inset of Fig. 6.11, the method of spatial separation of traps involved using two electrometers during TSC characterization. Traps located within the oxide were isolated by attaching the positive lead of the first electrometer to the MOSFET gate, and the negative lead to the source, drain, and body terminals. As a result, the measured TSC in the gate electrometer was due to detrapping between the top of the polysilicon gate and the bottom of the inversion layer.

The resulting TSC peaks at 55 K are presented in Fig. 6.11. At 20 K, when the negative gate field was changed to positive, the source and drain instantaneously provided a source of inversion electrons and the gate field terminated on the inversion layer. Regardless of the value of the warmup field, i.e., how strongly in inversion the device was biased, the magnitude of the TSC peaks remained between 4 and 5 pA. The measurement was repeated using a variable cooldown field ($E_{cooldown}$ = -2 to -5 MV/cm) and a constant warmup field (E_{warmup} = 2 MV/cm). The resulting peaks, not shown here for brevity, were virtually identical to those shown

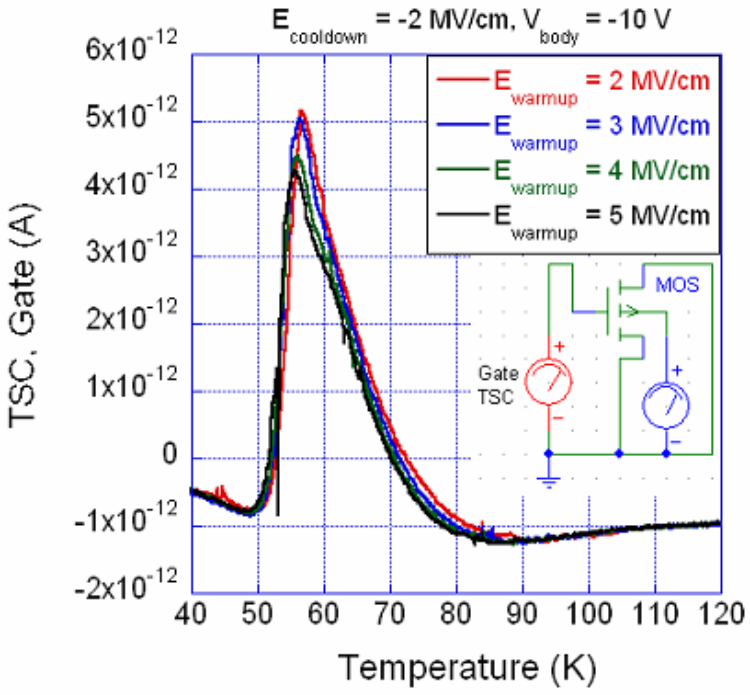

Figure 6.11: An n-channel 4H-SiC MOSFET biased in accumulation during cooldown and inversion during warmup.

in Fig. 6.11. Therefore, the density of the hole accumulation layer during cooldown also did not influence the magnitude of the TSC peaks. Using eq. 1, a trap density of 4.87x10^{11} cm^{-2} was calculated for the 2 MV/cm curve in Fig. 6.11.

Next, we varied the body bias while keeping the gate field constant. The field induced by V_{body} was separated from the oxide by the same inversion layer that separated the oxide peaks in Fig. 6.11. The TSC spectra from the body-connected electrometer are provided in Fig. 6.12.

During warmup, the positive gate field terminated on the inversion layer, which had formed instantaneously at 20 K, as was the case in Fig. 6.11, and naturally the gate electrometer registered the same 55 K peaks as before (not shown to avoid re-

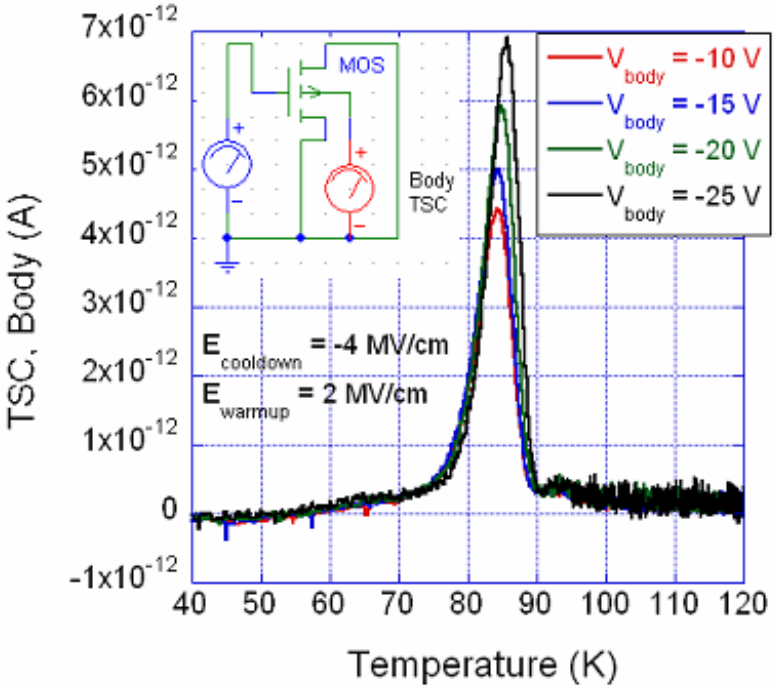

Figure 6.12: TSC spectra of an n-channel 4H-SiC MOSFET biased in accumulation during cooldown and inversion during warmup. The TSC spectra were measured from the body of the MOSFET, with a variable V_{body} bias applied by the electrometer.

dundancy). The negative body bias drew positive charge from beneath the inversion layer, which resulted in TSC peaks around 85 K.

In summary, the result of having two separate local electric fields within the device was the separation of the spatial origin of the 55 K and 80 K peaks. However, this technique was insensitive to the different types of traps emitting from a given region. Curiously, detrapping from hole traps occurred at the same temperature as detrapping from Al acceptors, as observed from the excess trap concentration near 80 K in Fig. 6.9. Assuming an Al activation energy of 0.23 eV, a capture cross of

$\sigma_{P,80K}$ = 4.02 x 10^{-14} cm^2 was obtained for emission peaking at 80 K [102]. The method for separating of the 80 K peak into its constituent types of traps is the subject of the next section.

6.2.2.2 Energy Separation of Carrier Traps Near 80 K (γ-ray irradiation method)

In the previous section we observed that the density of traps emitting near 80 K could not be accounted only by the acceptor concentration of the samples. We concluded that there was an additional trap present at an overlapping energy level, and determined it to be a hole trap. In this section, we support this hypothesis used a γ-ray irradiation technique to separate the two types of traps in the TSC spectra.

Two MOS capacitors with TSC spectra identical to those shown in Fig. 6.8 and 4 were irradiated with a total dose of 100 krad dose using a ^{60}Co source. During irradiation, one capacitor was biased in depletion with 2 MV/cm gate field (sample A), whereas the other capacitor was biased in accumulation with -2 MV/cm gate field (sample B). The high-frequency C-V characteristics of the devices before and after irradiation were measured at room temperature and presented in Fig. 6.13.

The more negative shift in flatband voltage for sample A indicated that the radiation-induced positive net oxide charge was closer to the SiO_2/SiC interface due to the positive field during irradiation of sample A. Conversely, the negative gate field during irradiation of sample B caused the oxide charge to be pulled away from the interface, thus inducing a lower flatband voltage shift.

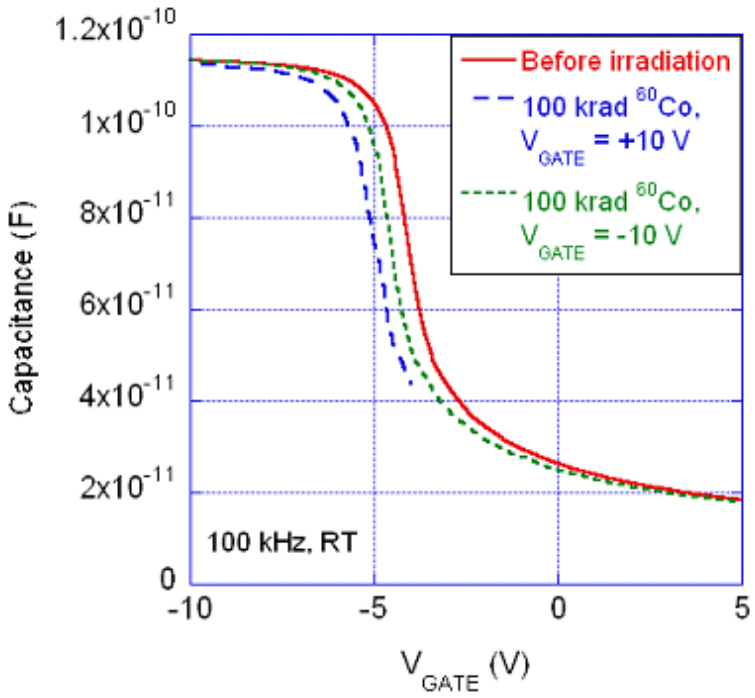

Figure 6.13: Post gamma-ray irradiation room-temperature high-frequency C-V characteristics of a p-type epitaxial 4H-SiC MOSCAP.

While further experiments are necessary, we believe the absence of TSC peaks at 55 K in Fig. 6.14 suggested that the gamma-irradiation had emptied any oxide traps isolated by the localized electric field method described above. On the other hand, emission from the 80 K range was distinctly different for the two samples. The 80 K peaks in Fig. 6.14a (sample A) did not depend on the cooldown field after irradiation, suggesting emission from a fixed density of charge in the epitaxial region. Integration of the 80 K peaks in Fig. 6.14a using eq. (1) produced a trap density of 9.05×10^{15} cm^{-3}, which was very close to the nominal Al doping level of 1×10^{16} cm^{-3}. Identical measurements under 0 V warmup bias caused this trap density do decrease by about 50 %, suggesting that ionization of Al dopants was

assisted by the positive gate field.

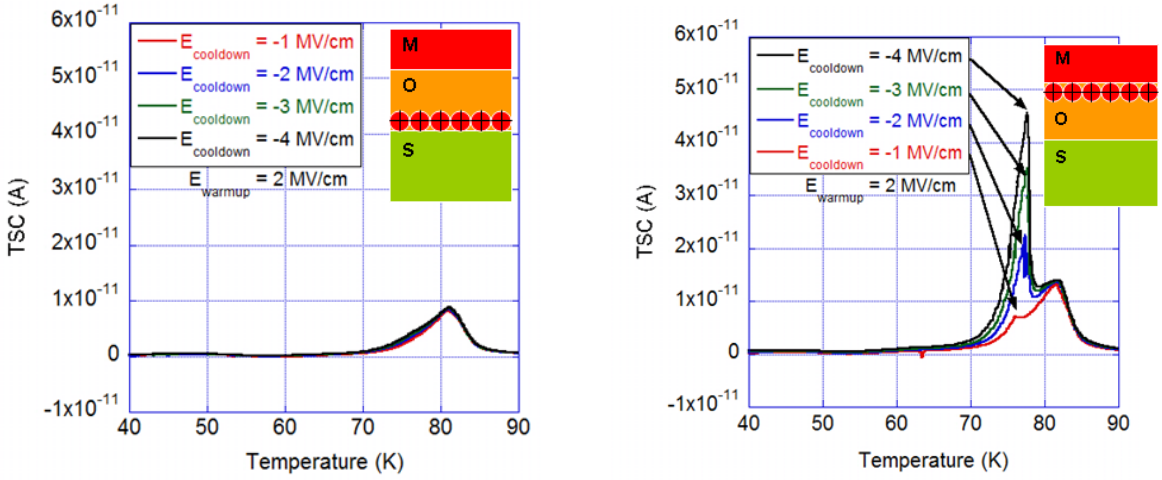

Figure 6.14: Post gamma-ray irradiation TSC spectra of a p-type epitaxial 4H-SiC MOSCAP biased in accumulation during cooldown and depletion during warmup with a constant warmup field E_{warmup} = 2 MV/cm. The gate bias during irradiation was a) 2 MV/cm and b) -2 MV/cm.

The TSC spectra for sample B, shown in Fig. 6.14b, illustrated the effect of the negative gate field during irradiation. While the TSC spectra of sample A (Fig. 6.14a) suggested that the hole traps were filled by the radiation-induced charge, the shift of this charge away from the interface in sample B lowered the potential barrier, causing emission from the hole traps to be observed at a slightly lower temperature (about 77 K). The emission from the acceptor states near 80 K was nearly identical in magnitude to that observed in Fig. 6.14b. One could thus subtract the acceptor state density calculated from Fig. 6.14a from the total trap density calculated from the 80 K peaks in Fig. 6.9 to estimate a field-dependent hole trap density of $N_{t,hole}$ = 2.08x10^{15} cm^{-3} at 2 MV/cm gate field and $N_{t,hole}$ =

$2.5x10^{16}$ cm^{-3} at 4.5 MV/cm gate field (as plotted in Fig. 6.10).

As a result, we have not only separated the origin of the 55 K and 80 K peaks from different regions of an MOS device using the localized field technique, but we have also separated the trapping mechanisms comprising the 80 K peaks using a γ-ray irradiation technique.

6.2.2.3 TSC Spectra of MOSFET Source/Body n^+-p Junction

Another way to verify that the 55 K peaks were due to traps located within the oxide (or the polysilicon) was to obtain TSC spectra from electric field which was a) localized to regions of the device where neither oxide nor poly-Si were present and b) not terminated on a SiO_2/SiC interface. This configuration was achieved by connecting an electrometer to the source-body n^+/p junction of the MOSFET, while leaving the other device terminals floating. Room temperature current-voltage measurements were performed on the junction after each TSC measurement cycle. During cooldown, the junction was weakly forward biased (1 nA forward current at 2.5 V bias). During warmup, the junction was reverse-biased from V_{rev} = -20 V to -100 V, which produced the TSC spectra shown in Fig. 6.15.

It could be seen that the magnitude of the 50-55 K peaks was negligible compared to those in Fig. 6.11. Their presence was attributed either to residual nitrogen donors present during epitaxial growth and compensated by the Al acceptors, or to oxide traps located in the gate overlap regions. This result supported the hypothesis that the origin of the 50 K peaks was in states not physically located in the epitaxial

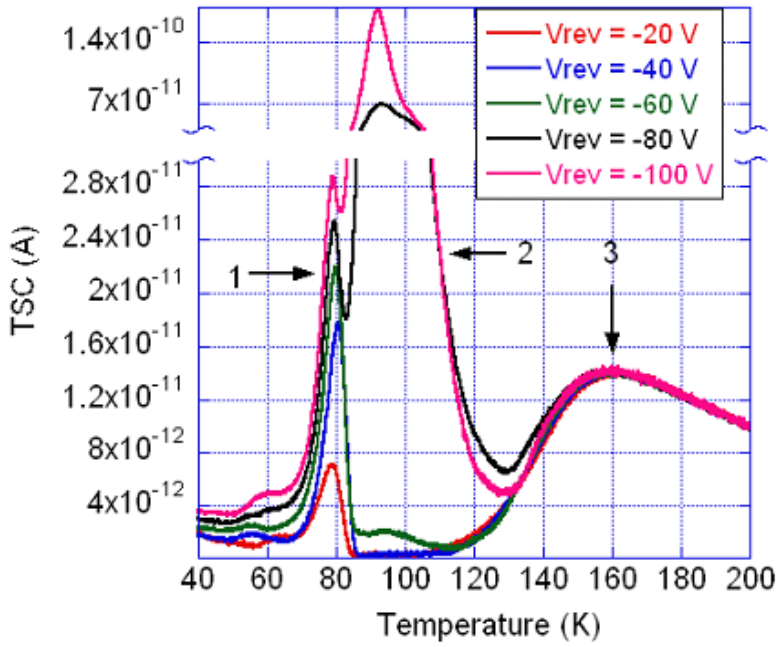

Figure 6.15: TSC spectra of the source-body n^+-p junction of an n-channel 4H-SiC MOSFET with the gate and drain of the device floating.

SiC.

The temperatures at which significant TSC was observed were 80 K (group 1), 90-100 K (group 2), and 160 K (group 3). The respective trap densities calculated using eq. 6.2 from TSC curves measured at V_{rev} = -100 V were $N_{t,1}$ = 2.25x10^{17} cm^{-3} (5.62x10^{13} cm^{-2}), $N_{t,2}$ = 3.45x10^{18} cm^{-3} (8.62x10^{14} cm^{-2}), and $N_{t,3}$ = 2.38x10^{18} cm^{-3} (5.95x10^{14} cm^{-2}).

The three TSC peak groups varied differently with bias. The magnitude of the group 1 peaks increased with reverse bias, from -7 pA at V_{rev} = -20 V to -28 pA at V_{rev} = -100 V. This behavior was consistent with the hypothesis that TSC peaks around 80 K were partially caused by the Al acceptor states. Their spatial

distribution in the depletion region suggested that as it expanded due to the higher reverse bias, more acceptor states would be located in the space charge region, and the magnitude of the resulting TSC peak would be higher.

TSC peaks in group 2 were not observed at low reverse biases (-20 V and -40 V). A small peak of about 2 pA was observed at 95 K at V_{rev} = -60 V. At high reverse biases (V_{rev} = -80 V and -100 V), this peak split into two peaks at 93 K and 105 K, and their maximum current levels increased by about two orders of magnitude. The magnitude of the 93 K peak was 175 pA at -100 V reverse bias. The depletion region width, calculated at about 3 um for this peak, suggested that the group 2 peaks were due to either substrate defect states or implantation damage deep into the epilayer.

Independent of the reverse bias applied to the source/body junction during warmup, the group 3 peaks maintained a constant magnitude of about 14 pA. However, increasing the forward bias during cooldown (2.0 V, 2.5 V, and 3.0 V) caused their magnitude to increase. Therefore, the diffusion current in forward bias during cooldown might have caused carriers to trap into defect states in the space charge region, where the diffusion current density was high. The peaks' constant magnitude at variable depletion width in reverse bias during warmup indicated that the spatial distribution of these defect states did not extend far away from the space charge region.

Based on the TSC data presented in this work, the two TSC peaks observed on SiO_2/SiC structures were attributed to traps in the oxide (55 K peak) and to Al acceptor ionization and hole traps near the interface (80 K peak). Lysenko

and Ólafsson (Ref. [169] and [170], respectively) observed for the case of 6H-SiC a dependence of the 40 K peak on the accumulation field. In our work, this dependence was observed for the 80 K peak in 4H-SiC (e.g., Fig. 6.9). Additionally, unlike the conclusion made by Lysenko, our data suggested that the hole traps emitting near 80 K were on the epitaxial side of the interface, rather than on the oxide side.

6.3 Chapter Summary

We have described heterojunctions between both p-type and undoped NCD films and n- and p-type 4H-SiC epitaxial layers. A highly rectifying behavior with low turn-on voltages (< 1 V) was observed and possible mechanisms to explain this behavior were provided. I-V measurements yielded barrier heights of less than 0.85 eV for all samples. C-V measurements suggested larger barrier heights for the p^+ NCD / p^- SiC and undoped NCD / n^- SiC samples possibly due to the presence of defects in p^- SiC and surface hole accumulation in undoped NCD. Our results suggested that NCD films should be ideal high-temperature surface-passivating contacts that may be used for both electrical and optical characterization of defects in SiC epitaxial films. As SiC power MOSFET devices continue to improve, better methods for high-temperature electrical and optical characterization will prove to be necessary.

Finally, we reported on the application of the thermally stimulated current method to study traps in n-channel epitaxial 4H-SiC MOSFET devices. TSC spectra were first observed in p-type MOS capacitors near 55 K and 80 K. The same spectra

were measured on MOSFET devices and spatially separated by utilizing electrical connections which applied separate electric fields to the oxide and bulk regions of the device. The 55 K peaks were attributed to charge in the oxide or its interface with the polysilicon layer. Using γ-irradiation, we determined that emission near 80 K was contributed by Al acceptor ionization and hole traps in the SiC epilayer near the SiO_2/SiC interface. After irradtiation, the contributions from these two sources can be split into two peaks. Previous studies of MOS capacitors on 6H-SiC observed TSC spectra at similar temperatures. Defects in the source-body n^+-p junction confirmed the presence of peaks due to Al acceptor states, and suggested the presence of implantation damage near the metallurgical junction, as well as defects near the n^+ SiC substrate.

Chapter 7

Conclusions and Future Research Possibilities

This dissertation has presented a number of paths in wide bandgap semiconductor device research. AlGaN/GaN HEMT devices were developed to address several pressing issues in power switching device development: normally off operation, surface passivation, and reduction of self-heating effects. A natural goal then presents itself in the realization of an in-situ passivated, enhancement-mode, low self-heating HEMT that marries the different HEMT fabrication approaches developed in Chapters 2, 3, and 4. Specifically, the three-year HEMT development program at NRL targets 1200 V operation at 10 times the switching frequency of Si devices (f>10 MHz), while reducing the on-state resistance 10-fold ($R_{ON} < 5$ mΩ-cm^2) and the input and output capacitances 5-fold.

The power switching performance will be best characterized by operating the fabricated devices in one of their primary targeted applications: a boost converter. Figure 7.1 and 7.2 show the boost converter circuit and our testing setup. The board is mounted directly onto a wafer probing card so that devices can be tested at the wafer level. This approach avoids the need to package individual devices for testing and greatly speeds up the characterization process. Figure 7.3 shows sample switching characteristics of the boost converter setup, measured using an in-situ SiN_x passivated HEMT.

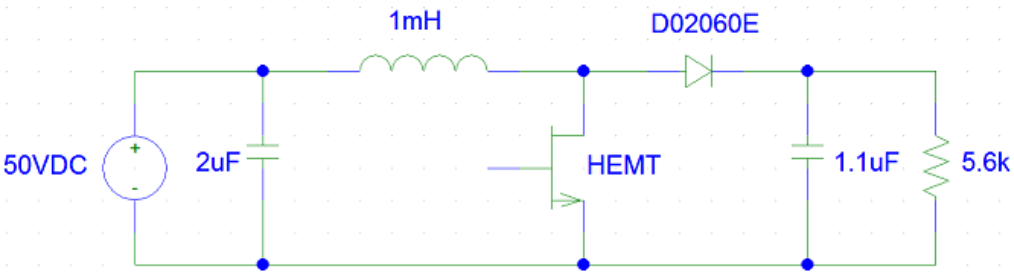

Figure 7.1: Boost converter circuit used for testing HEMT devices.

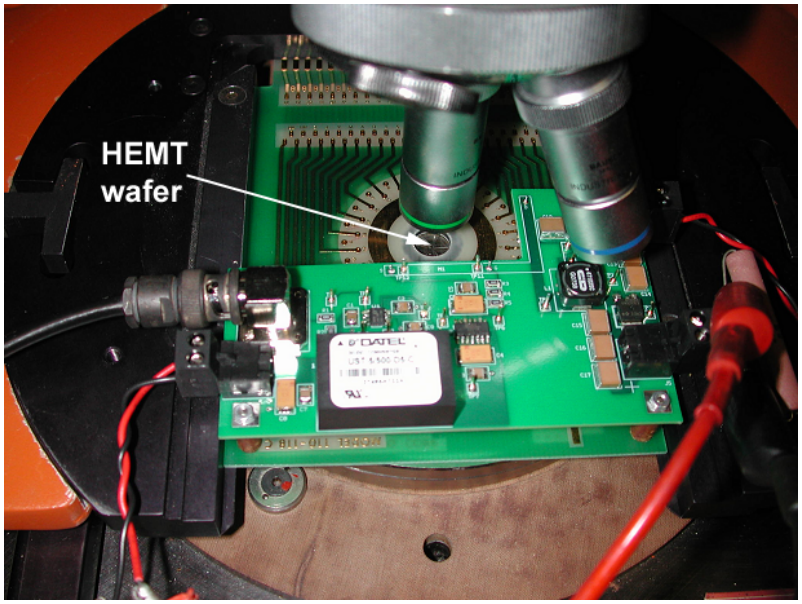

Figure 7.2: Probe card with a boost converter mounted on a probe station to test HEMT devices on the wafer level.

Nanocrystalline diamond has been explored for its high thermal conductivity, UV transparency, and ability to form Schottky heterojunctions with 4H-SiC and interesting interfaces with Si and III-Nitrides. A metal-diamond-Si capacitor was compared to its SiO_2 counterpart for oxide charge. Ohmic contacts to NCD were demonstrated using different metals and annealing conditions. The NCD/4H-SiC

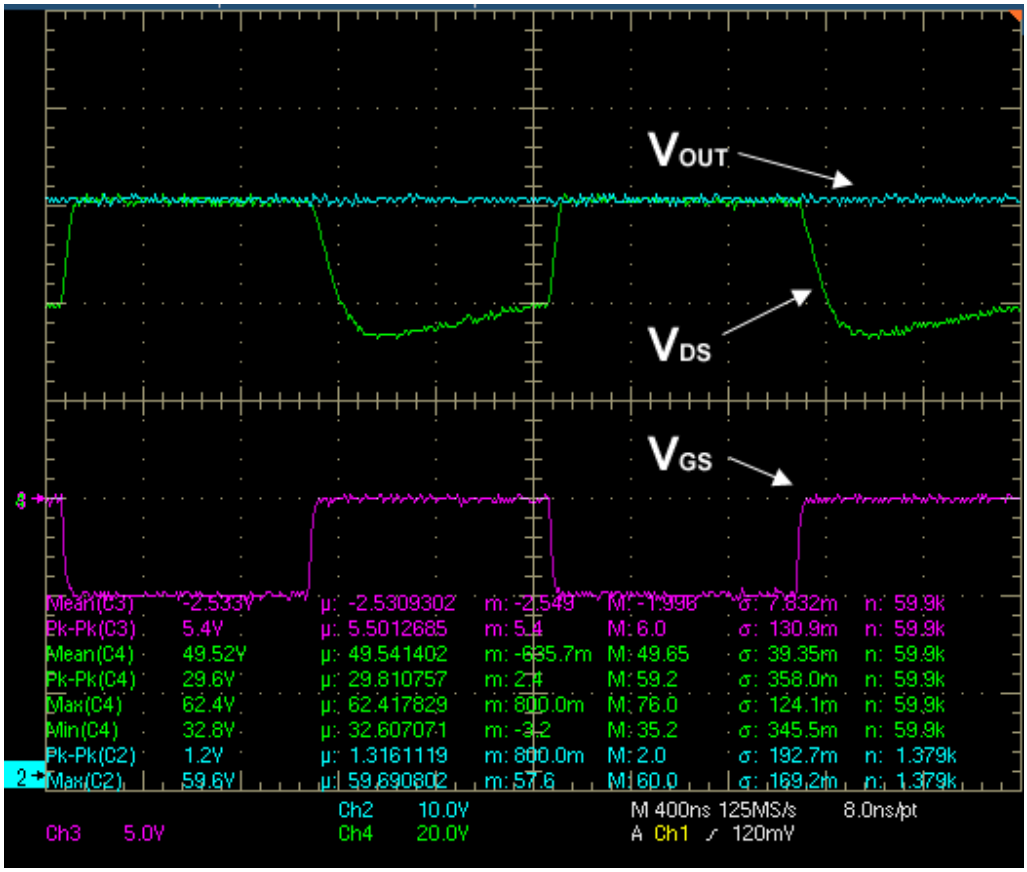

Figure 7.3: Input and output waveforms of the boost converter operating using an AlGaN/GaN in-situ passivated HEMT at 500 kHz and 50 % duty cycle.

heterojunction has been characterized using barrier height extraction methods, and trap assisted tunneling was proposed as a main conduction mechanism. To support this argument, deep level characterization in 4H-SiC epitaxial films was performed using thermally stimulated current methods. That research lead to the development of techniques for the spatial separation of defects in 4H-SiC transistors.

Appendix I

SEM Images of Device Processing Conditions

I.1 Thermal Stress of HEMT devices

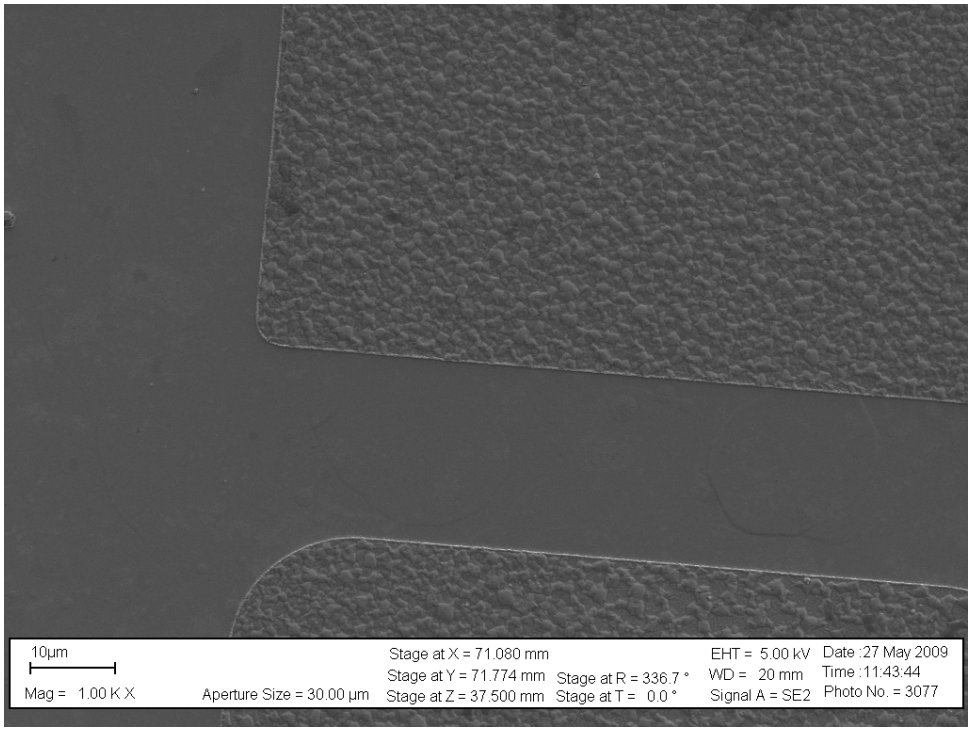

Figure I.1: Reference HEMT, annealed, 1,000x magnification

Figure I.1 shows the gate-drain spacing of an AlGaN/GaN HEMT after 5-hour anneal at 750 ℃. Visible on the image are the Ohmic contact metals and the AlGaN surface. No significant surface damage was observed, even though slight N desorption was expected at this temperature. The subsequently gated device showed comparable saturation current levels.

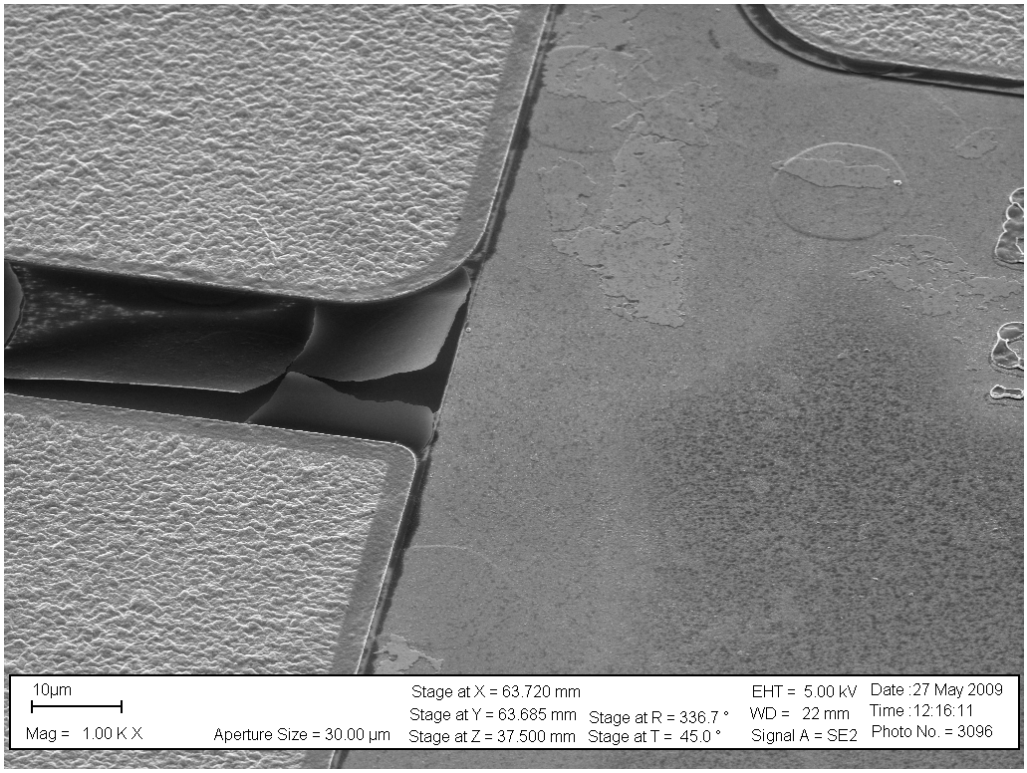

Figure I.2: HEMT with Al_2O_3, annealed, 1,000x magnification

Figure I.2 shows the gate-drain spacing of an AlGaN/GaN HEMT with 50 nm of ALD-deposited Al_2O_3. SEM imaging was performed after annealing at the same conditions as the reference HEMT above. Exfoliation of the Al_2O_3 layer was observed, and subsequent HEMT measurements showed no gate modulation.

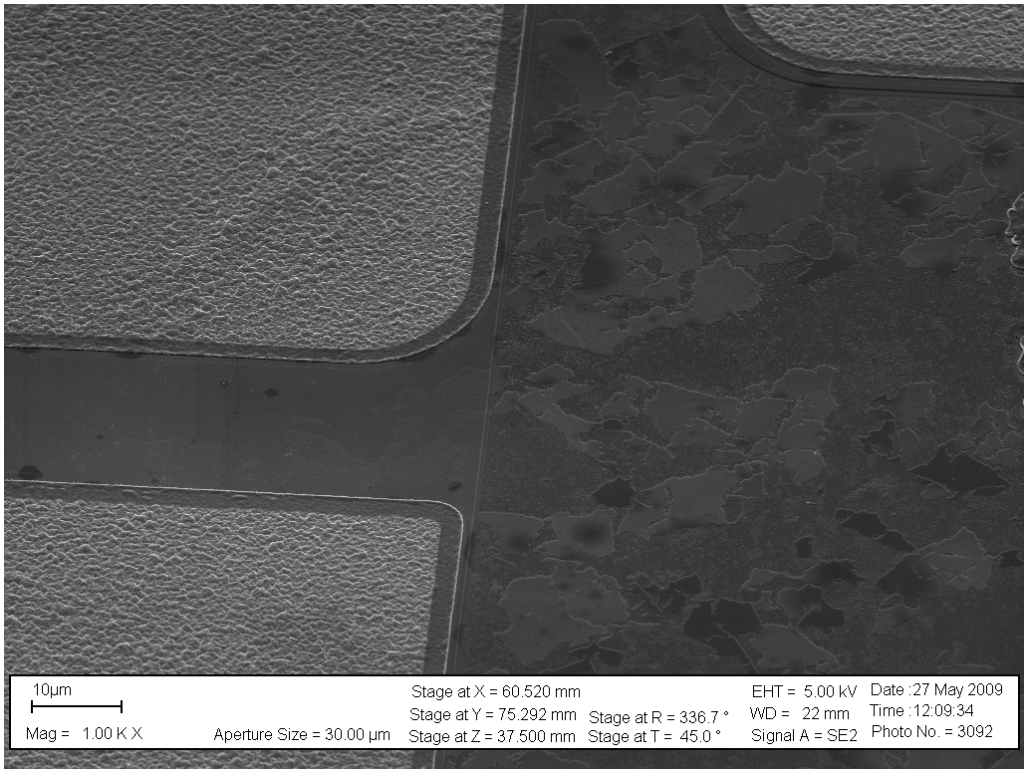

Figure I.3: HEMT with SiO_2, annealed, 1,000x magnification

Figure I.3 shows the gate-drain spacing of an AlGaN/GaN HEMT with 50 nm of PECVD-deposited SiO_2. SEM imaging was performed after annealing at the same conditions as the reference HEMT. The quality of the dielectric degraded significantly off the mesa, but in the channel no extensive damage was observed. Upon gate deposition, functional HEMT devices were observed, as previously reported in Chapter 5.

I.2 Nanocrystalline Diamond Etching

Following in this section are SEM micrographs of etched diamond in the gate region of the fabricated devices. Fig. I.4 below shows the gate area in the center. The recessed region where the diamond was etched is about 3 μm wide. The Ohmic contact is visible on the bottom left corner, as well as the via etched in the diamond. The image suggests discontinuity of the Ni/Au gate metal over the 0.5 μm diamond step. To ensure gate metal continuity on this sample, a second Ni/Au metal stack was intentionally misaligned about 1 μm to the right of the gate recess. While gate metal continuity was a major concern during fabrication, a total Ni/Au metal thickness of 220 nm was found to be sufficient.

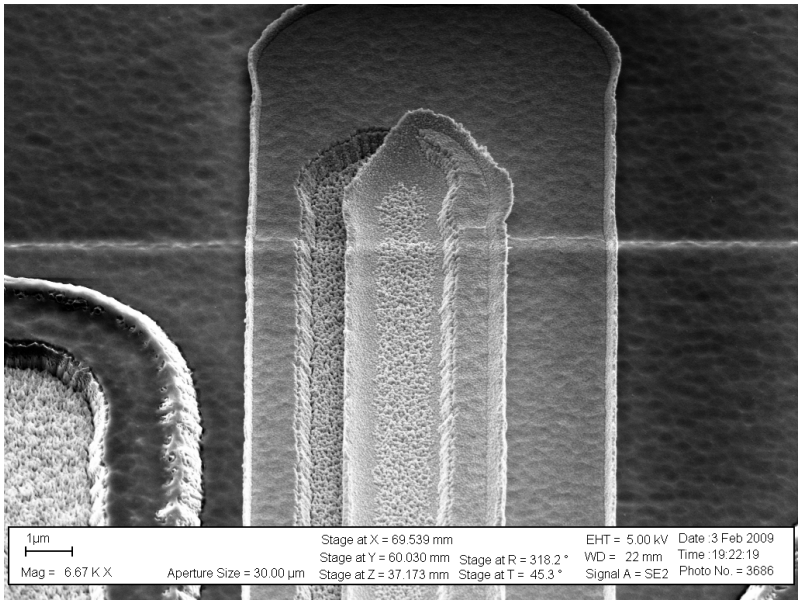

Figure I.4: HEMT with diamond, 8,000x magnification.

Figure I.5 shows a 20,000x magnification of the diamond HEMT gate area. The SiN_x etch mask on top of the diamond can be discerned, as well as the small

lip on the gate metal resulting from the lift-off process.

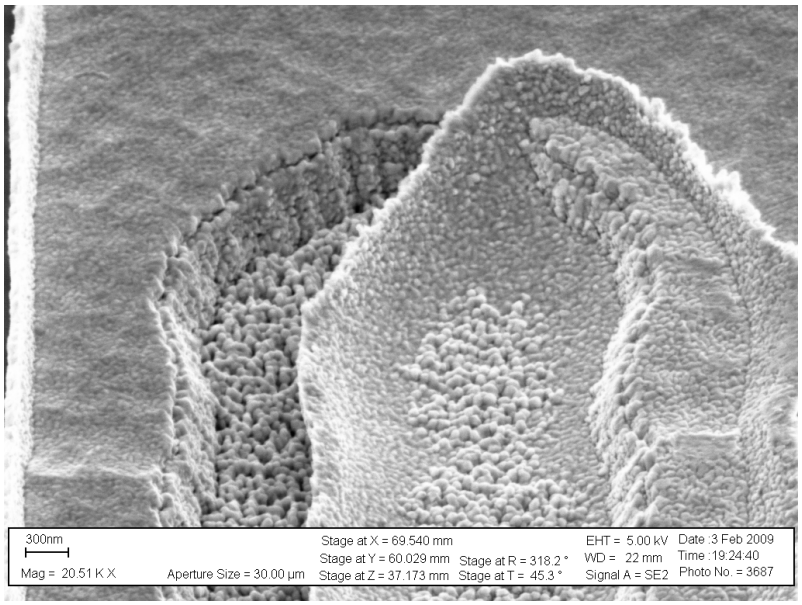

Figure I.5: HEMT with diamond, 20,000x magnification.

Figures I.6 to I.9 show SEM micrographs of NCD with a 100 nm thick SiN_x etch mask patterned on top of the NCD prior to etching. Magnification ranges from 8,000x to 30,000x.

Figures I.10 to I.11 show SEM micrographs of the NCD samples after etching for 60 minutes in O_2 plasma RIE at 200 W. The NCD layer appeared very rough, and the SiN_x etch mask was almost completely etched away. Clearly, this process was unacceptable, so an etch optimization study was performed.

Table I.1 lists the conditions for optimized ICP etching of NCD, compared to the 200 W RIE base etch process. Figures I.13 to I.16 present SEM images from the optimized NCD etch process. Condition E (Cl_2) was not imaged in SEM as the selectivity to the SiN_x etch mask was only 0.3.

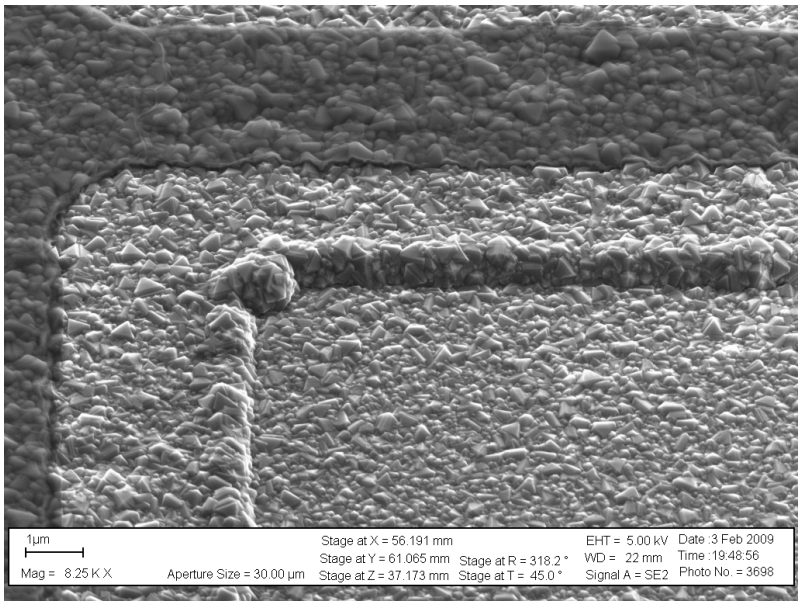

Figure I.6: Undoped diamond with a 100 nm thick SiN_x etch mask, before etching, 8,000x magnification.

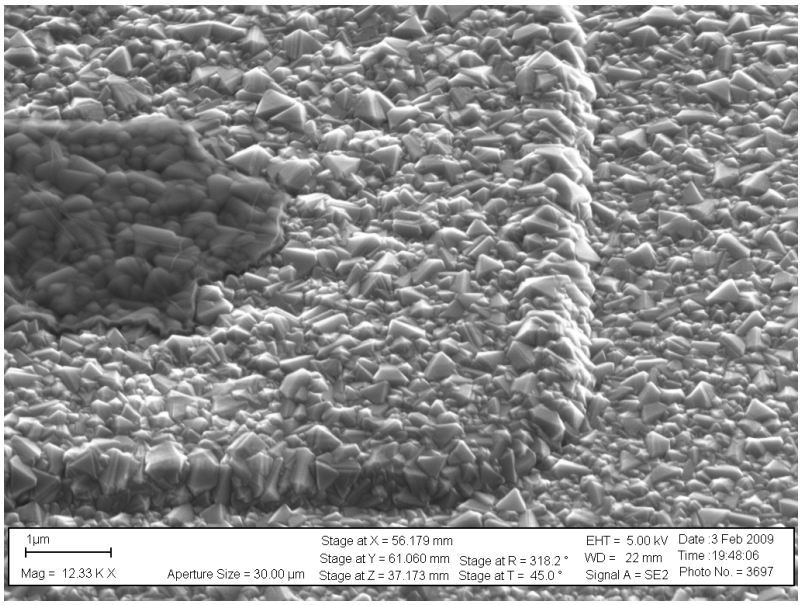

Figure I.7: Undoped diamond with a 100 nm thick SiN_x etch mask, before etching, 12,000x magnification.

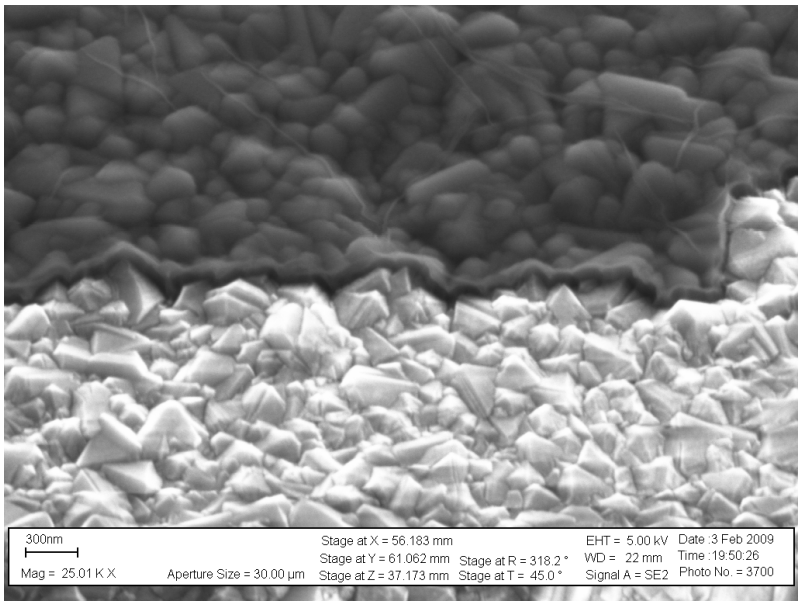

Figure I.8: Undoped diamond with a 100 nm thick SiN_x etch mask, before etching, 25,000x magnification.

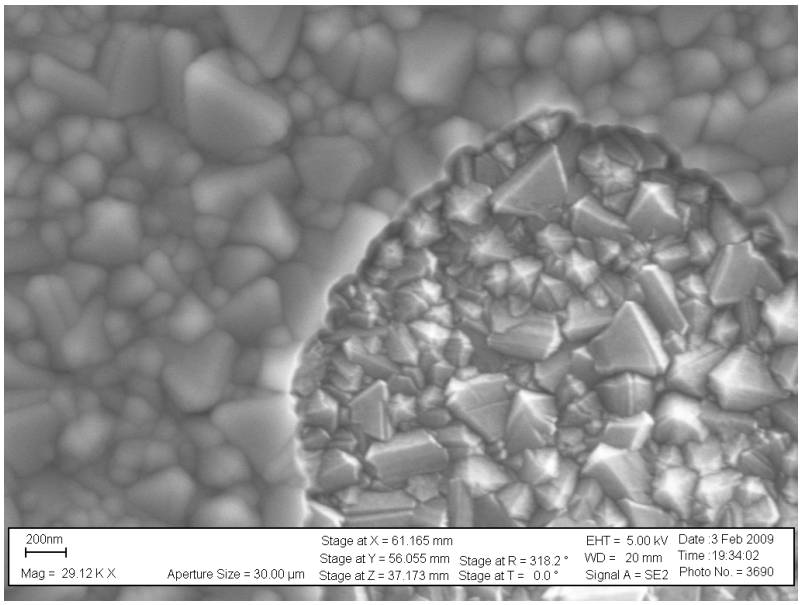

Figure I.9: Undoped diamond with a 100 nm thick SiN_x etch mask, before etching, 30,000x magnification.

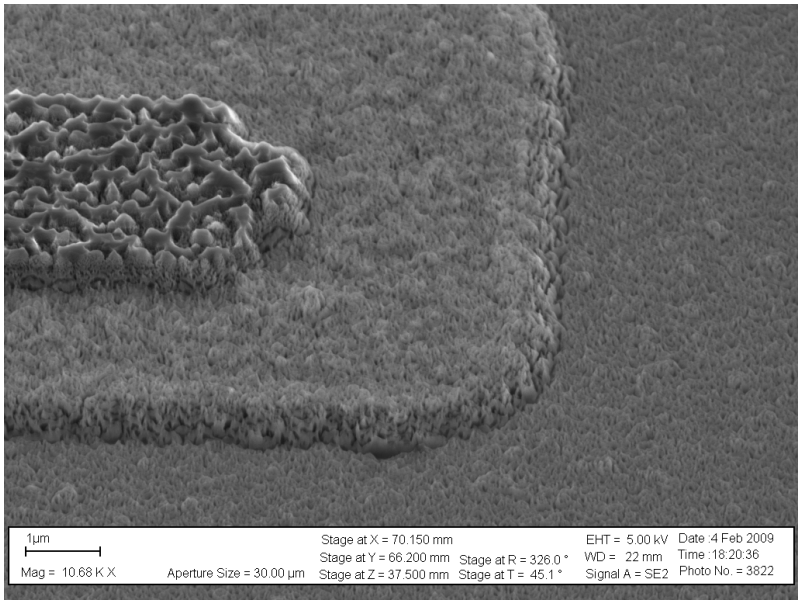

Figure I.10: HEMT with undoped diamond, after 60 min. of etching (O_2-RIE, 200 W), 10,000x magnification.

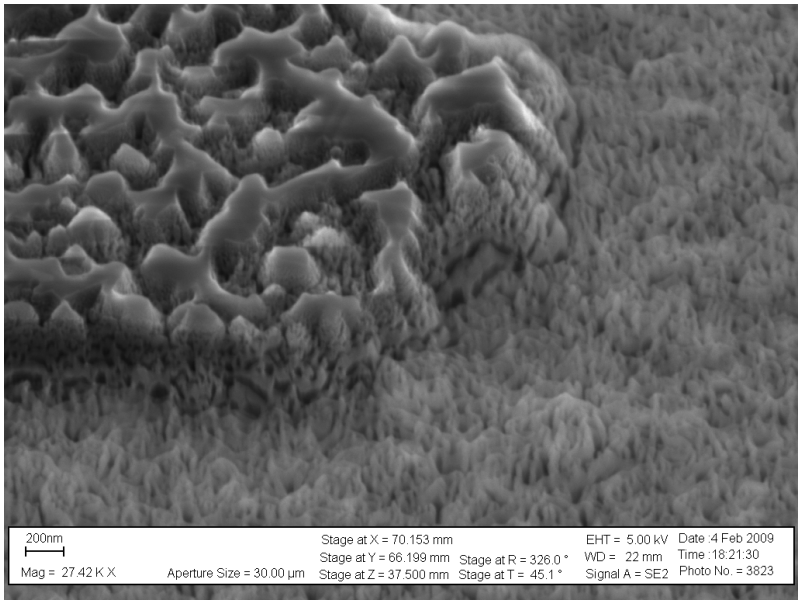

Figure I.11: HEMT with undoped diamond, after 60 min. of etching (O_2-RIE, 200 W), 27,000x magnification.

Table I.1: NCD etch optimization study.

Recipe	Chemistry	Power (ICP/RIE)	NCD Etch Rate (A/min.)	SiN_x Etch Rate (A/min.)	Selectivity
Base	O_2	200 W RIE	65	N/A	N/A
A	O_2/Ar	800/300	1900	250	7.5
B	O_2	1000/100	1950	225	9
C	O_2/CF_4	1000/100	1850	800	2.5
D	O_2 O_2/CF_4	1000/100 200/0	1800 60	800 60	2.5 1
E	Cl_2	900/300	300	>1000	<0.3

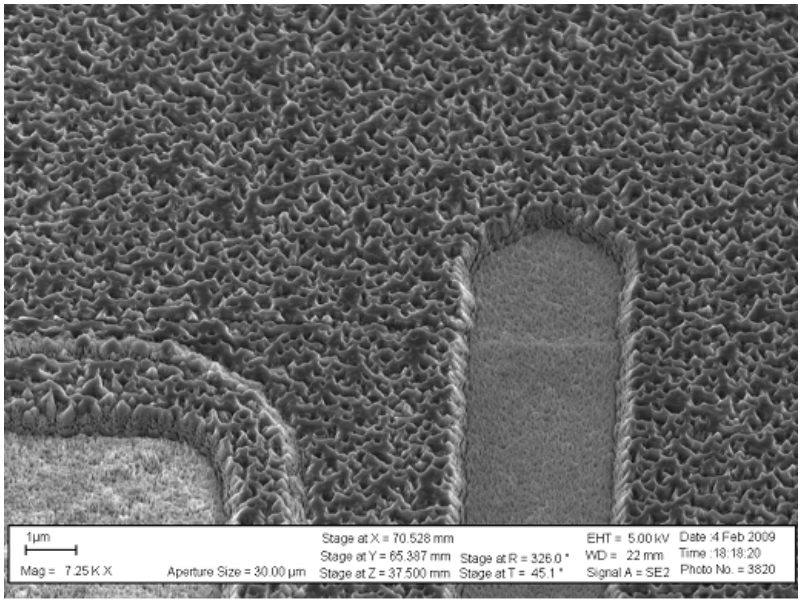

Figure I.12: Base process (RIE 200 W).

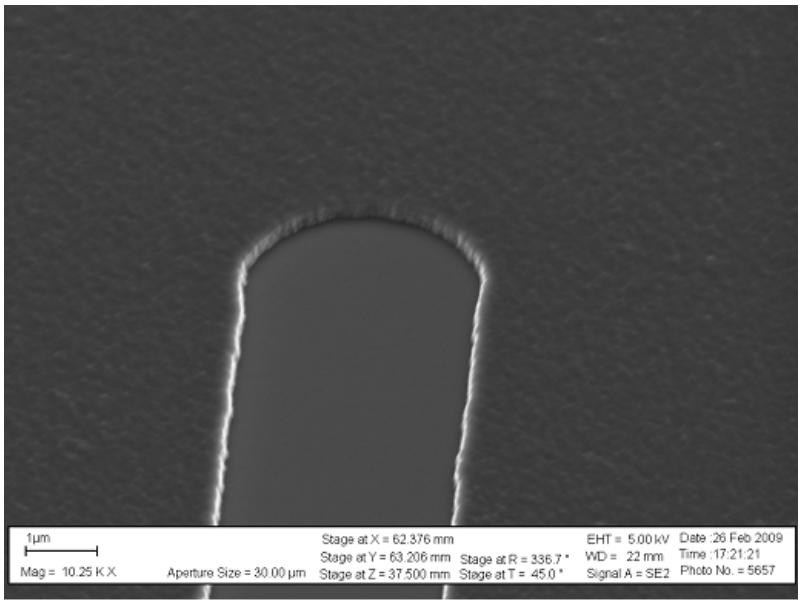

Figure I.13: ICP condition A: O_2/Ar, 800 W ICP, 300 W RIE power.

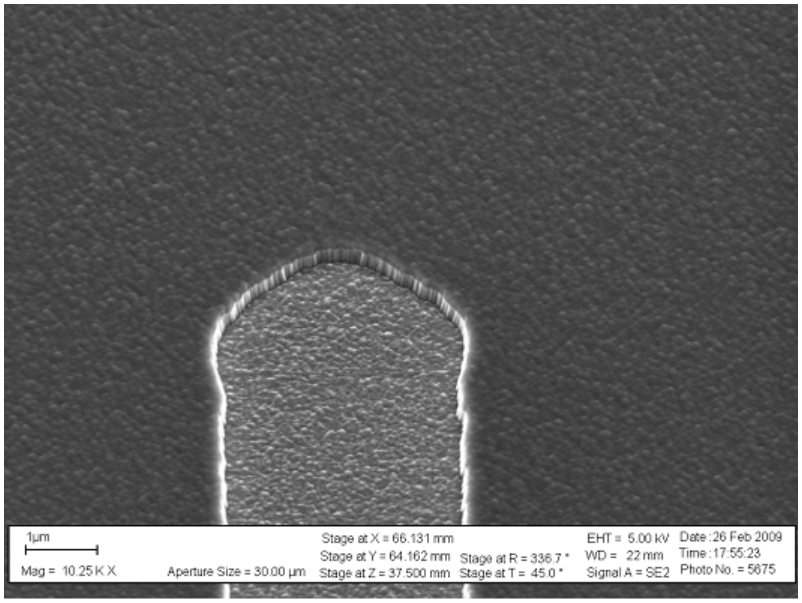

Figure I.14: ICP condition B: O_2, 1000 W ICP, 100 W RIE power.

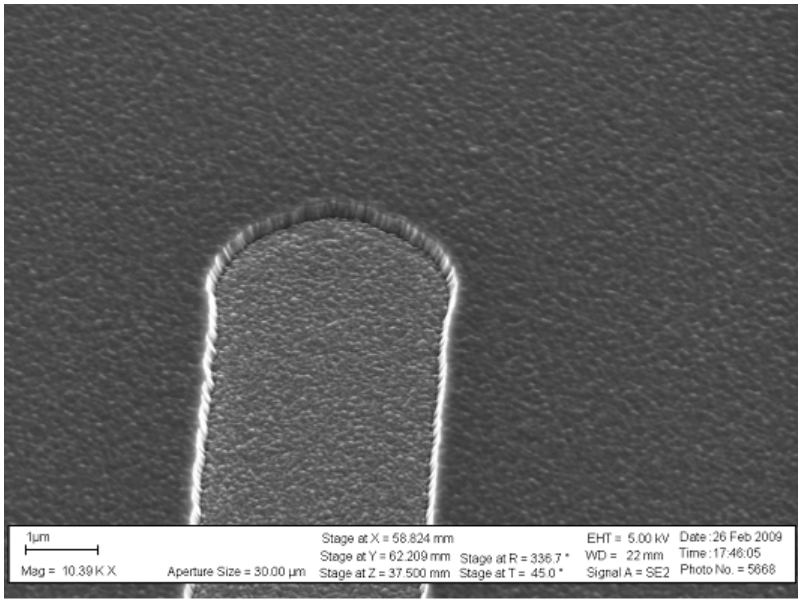

Figure I.15: ICP condition C: O_2/CF_4, 1000 W ICP, 100 W RIE power.

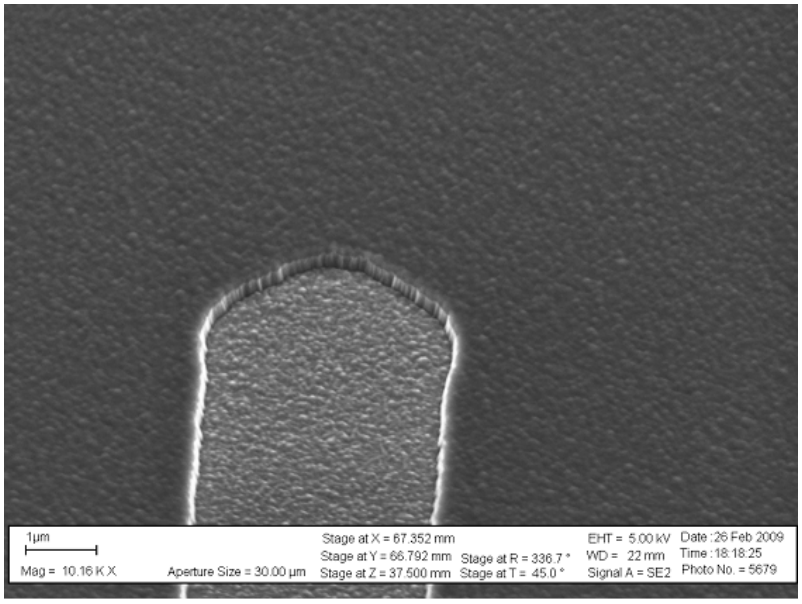

Figure I.16: ICP condition D: O_2 plasma (1000 W ICP, 100 W RIE) followed by O_2/CF_4 plasma etch (200 W ICP, 0 W RIE).

I.3 Liftoff Process for Ohmic Contacts to AlGaN/GaN

As Ohmic contacts are an integral part of semiconductor devices, a reliable process is required for their fabrication. For contacts to n-GaN and n-AlGaN, as described in Section 2.1.2, the traditional choice for metals has been Ti/Al/Ni/Au, with total stack thickness ranging between 2000 Å and 3100 Å. Deposition of four metals to such a thickness necessitates a lift-off process. Lift-off processes rely on the formation of a negative-slope resist profile using optical lithography. Upon deposition of the metals, the area under the negative resist slope (a.k.a., the lip) will cause a discontinuity in the metal layer, which makes removal of the unwanted resist and metal much easier.

To develop a lift-off process, four resists were considered: Shipley 1811 soaked in cholorobenzene, Futurex negative resist, AZ 5214 in negative-resist processing conditions, and a lift-off dual-resist LOR/1811 stack. The process is outlined below:

1. Dehydration bake on a hot plate for 2 min. at 190 ℃.
2. Spin LOR-10B resist for 60 s at 3000 rpm.
3. Bake on a hot plate for 5 min. at temperatures ranging from 150 ℃ to 190 ℃ (see Table I.2).
4. Spin Shipley 1811 positive resist for 30 s at 4000 rpm.
5. Soft-bake sample on a hot plate for 75 s at 105 ℃.
6. MUV expose (MJB3 aligner) for either 20 s or 30 s (see Table 7).

7. Develop either in 4:1 AZ400K:H_2O developer solution or MF312CD-27 developer for times outlined in Table I.2.

Scanning electron microscope (SEM) micrographs were obtained on features from all of the samples listed in Table 7. The best two in terms of achieved undercut profile are shown below. Sample D had resist undercut of about 1.4 μm, whereas Sample E had only 402 nm of undercut.

To achieve even smaller vertical undercut distances, LOR 5A resist was employed in processing as well. The process for an LOR 5A / S1811 resist stack is outlined below:

1. Dehydration bake on a hot plate for 2 min. at 190 ℃.
2. Spin LOR-5A resist for 10 s at 500 rpm, followed by 60 s at 4000 rpm. Make sure entire sample is covered with resist prior to spinning.
3. Bake on a hot plate for 5 min. at 190 ℃.
4. Spin Shipley 1811 positive resist for 30 s at 4000 rpm.
5. Soft-bake sample on a hot plate for 90 s at 105 ℃.
6. MUV expose (MJB3 aligner) for 60 s.
7. Develop in MF312CD-27 developer for 80 s
8. Perform O_2 de-scum process at 10 W RF power for 2 min.
9. Immediately before metallization, etch for 15 s in diluted HCl.

10. E-beam evaporate 200 Å Ti/2000 Å Al/400 Å Ni/500 Å Au.

11. Lift-off metals using acetone or photoresist stripper.

12. Rapid thermal anneal, 900 ℃, 30 s.

Table I.2: Results of LOR 10-B / S1811 liftoff processing experiments.

Sample Number	LOR 10-B Bake Temperature (℃)	MUV Exposure Time (s)	Developer Used	Total Development Time (s)	Comments
A	150	30	AZ400K:H_2O	28	Thin lines lifted off
B	150	30	MF312CD-27	25+5	Lots of lifting off
C	170	30	AZ400K:H_2O	30	
D	170	30	MF312CD-27	30	Some spots, pattern ok, undercut
E	180	30	AZ400K:H_2O	20+6	Spots cleared after addt'l 6 sec.
F	180	30	MF312CD-27	25+5	Some spots, pattern ok, undercut
G	190	30	AZ400K:H_2O	30	
H	190	20	AZ400K:H_2O	30+36	Clear
I	190	30	MF312CD-27	38	Thin lines lifted off

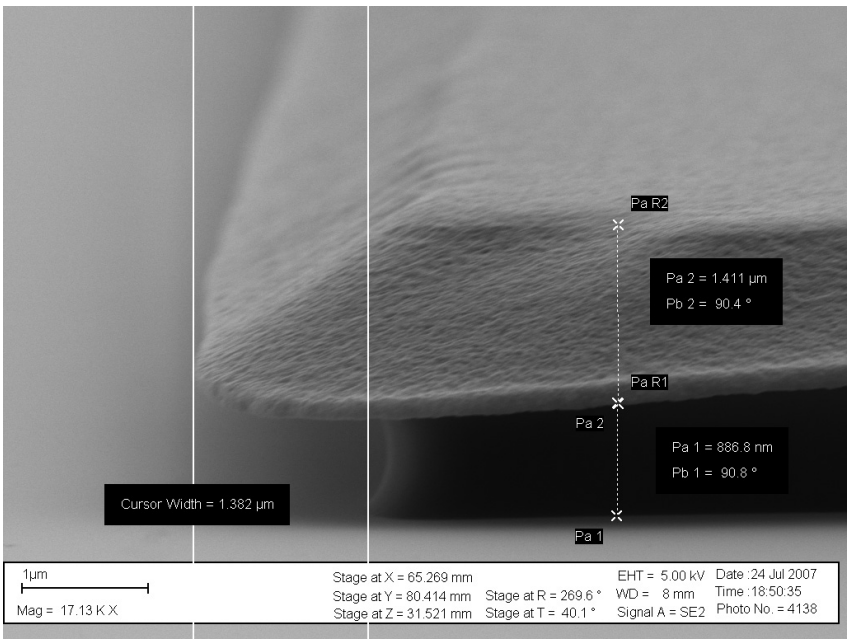

Figure I.17: Undercut profile of Sample D (LOR 10B / S1811).

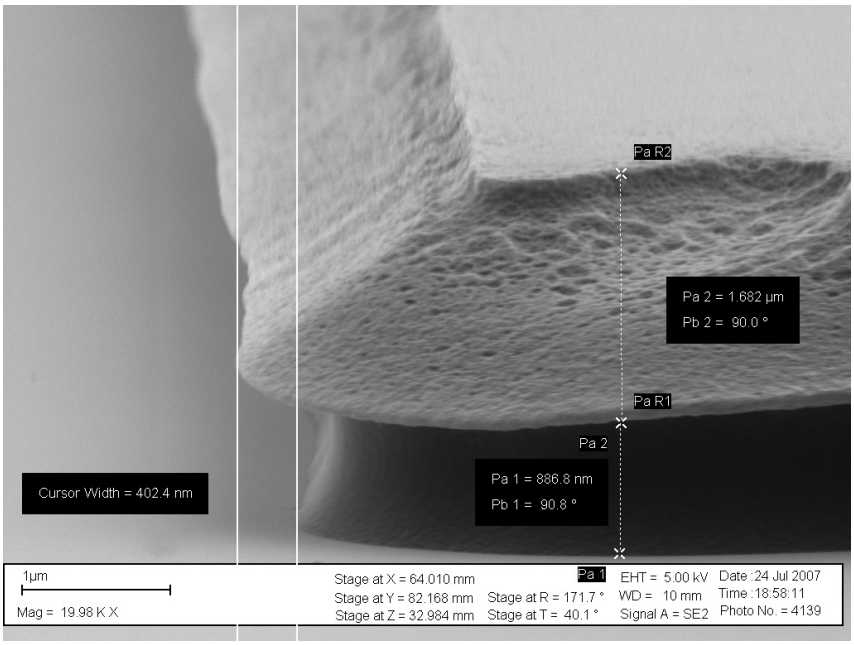

Figure I.18: Undercut profile of Sample E (LOR 10B / S1811).

Appendix II

Lithographic Masks

The processes described in Appendix I were performed with the following masks. The design was done with the LASI software package. Figure II.1 represents the complete reticle of devices and test structures.

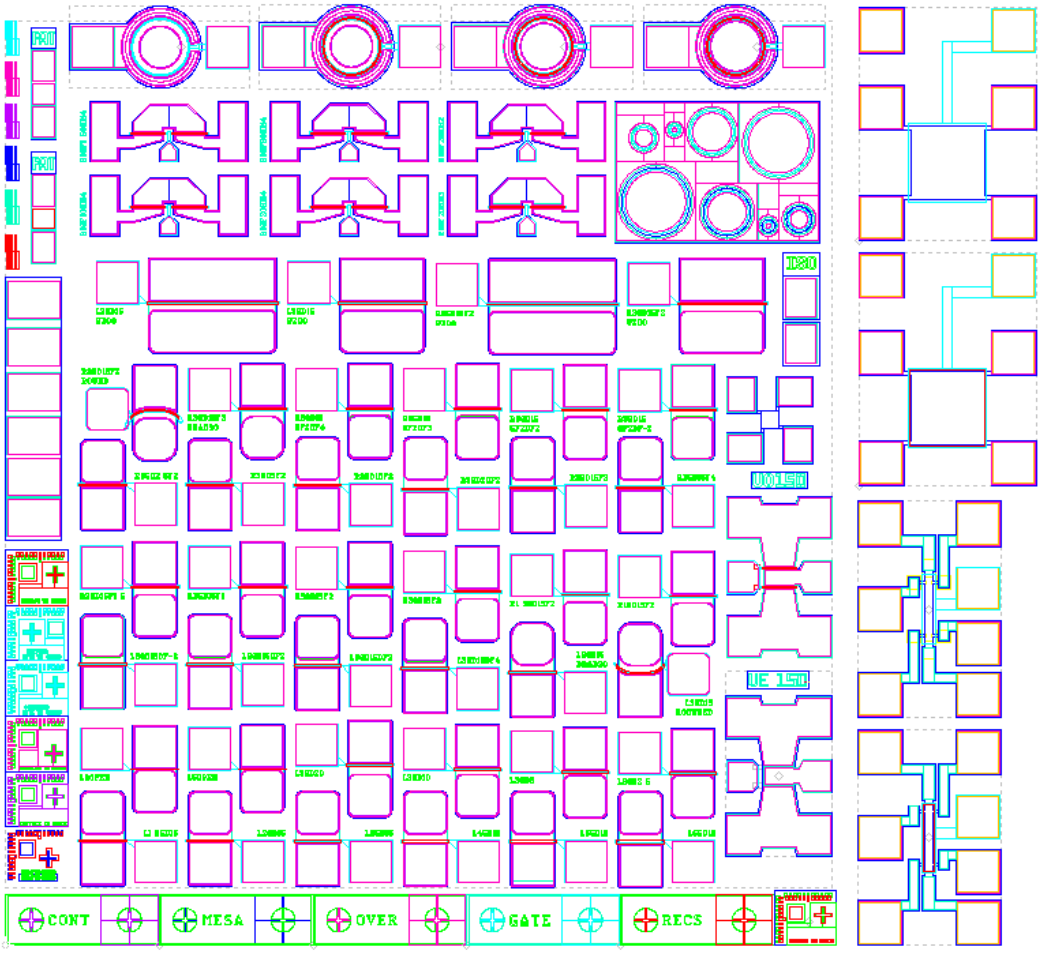

Figure II.1: HEMT mask reticle.

The device structures on the mask included forty lateral HEMT devices, four annular HEMTs, and eight microwave HEMTs. Detailed layouts of the lateral HEMTs are shown on Fig. II.2 and Fig. II.3. The recess region is shown on Fig. II.3 in red color. The other levels included the mesa region, the Ohmic and gate contacts, and the vias.

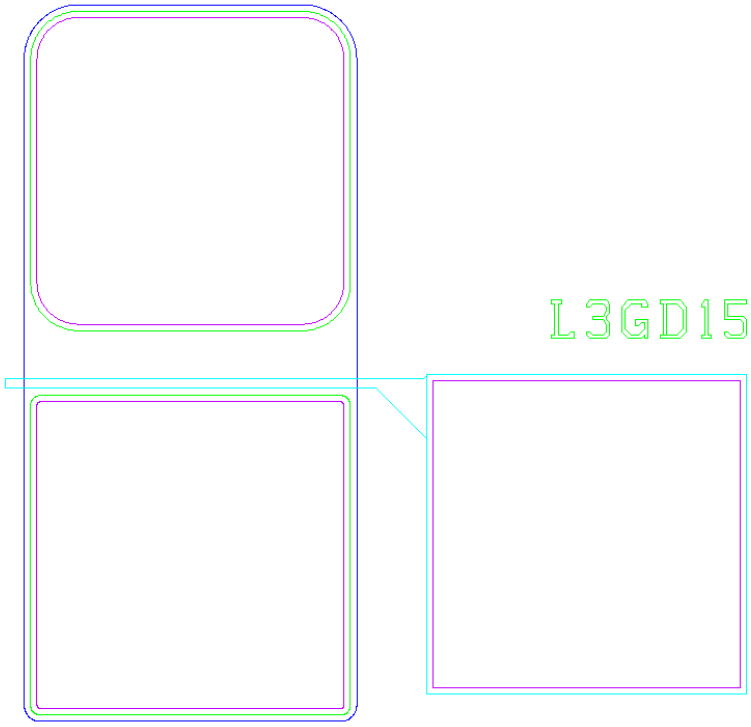

Figure II.2: HEMT layout without gate recess.

No two lateral HEMTs were the same: variables included gate length, gate-drain spacing, field plate length, and radius of the drain contact. Half of the lateral HEMT structures included a gate recess, as shown below. Two HEMTs were left without a gate for open-gate applications.

Figure II.4 shows a detailed layout of the annular HEMT. The recess region

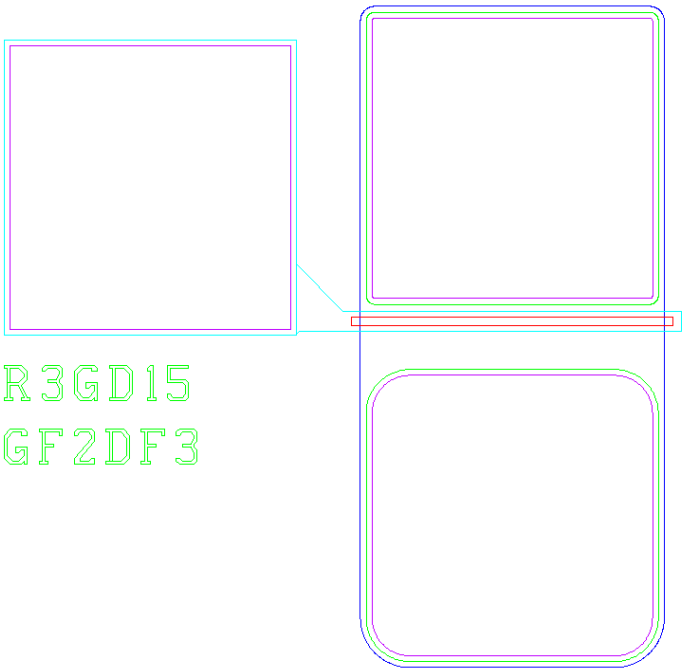

Figure II.3: HEMT layout with gate recess.

(not shown here) was present on three out of the four annular HEMTs on the mask.

The test structures consisted of one large-area testing HEMT (FATFET), a TLM structure for measuring sheet and contact resistance (Fig. II.5), a CV structure with and without mesa regions, Van der Pauw geometries with and without recess etch masks in the active area for mobility and sheet carrier density measurements, gated Hall structures, alignment marks (Fig. II.6 and II.7), and an indicator for resist development profiles (Fig. II.8).

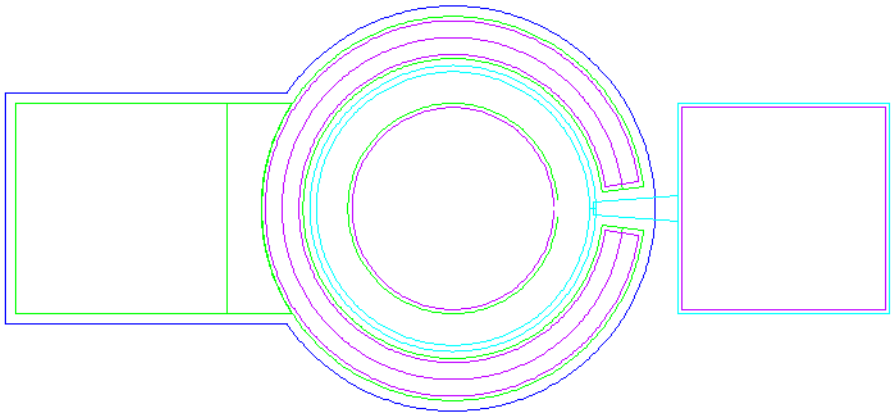

Figure II.4: Annular HEMT layout without gate recess.

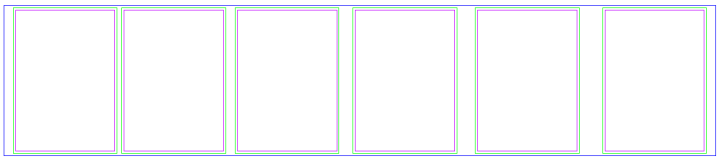

Figure II.5: Transfer length method patter for sheet and contact resistance characterization.

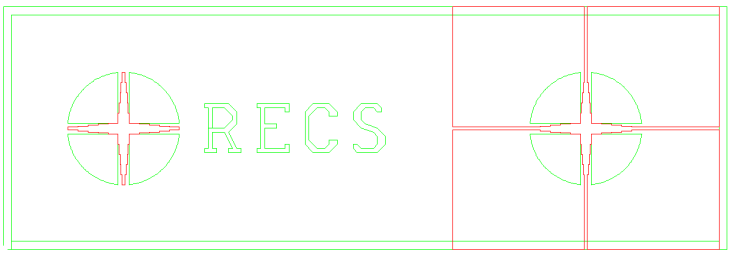

Figure II.6: Alignment mark.

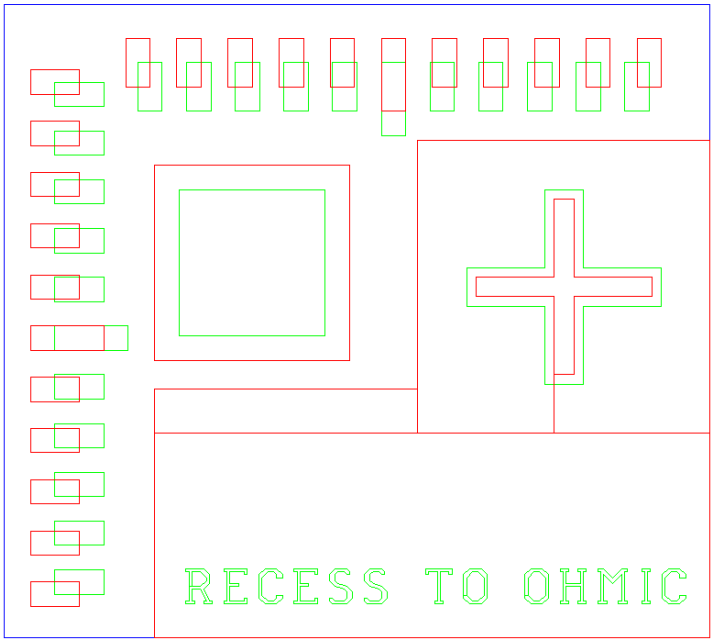

Figure II.7: Alignment mark.

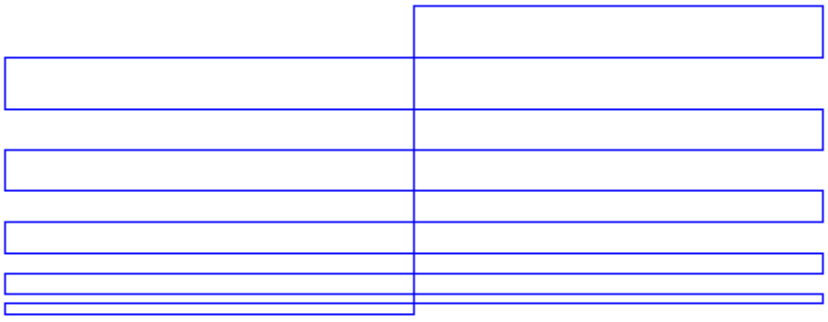

Figure II.8: Structure for evaluating resist development profiles.

Appendix III
Process Sheets
III.1 Process for HEMT with SiN_x passivation:

0. Wafer cleaning
    Acetone rinse
    IPA rinse and N_2 blow-dry
    1a. Lithography for mesa level (Note: Steps 1 and 2 are interchangeable)
    Spin S1818, 4000 RPM, 30s
    Bake at 105 ℃for 2 min. (hot plate)
    Expose for 70 sec.
    Develop in MF-319 for approx. 40-45 sec. with mesa mask
    DI rinse and N_2 blow-dry
    Post bake at 90 ℃for 10 min. (hot plate)
1b. Dry etch for mesa formation
    ICP Etch in Cl_2/Ar (10/5 sccm, 5 mTorr, 150 W ICP, 40 W RF), approx. 600 A/min
1c. Wafer cleaning Acetone soak 5 min
    Acetone spray/swab as-necessary
    IPA rinse and N_2 blow-dry
2a. Lithography for ohmic level
    Spin LOR7B, 4000 rpm, 30s
    Bake at 190 ℃for 5 min. (hot plate)
    Spin S1805, 4000 rpm, 30s
    Bake at 105 ℃for 1 min. (hot plate)
    Expose for 15 sec. at 15 mW/cm^2 with ohmic mask
    Develop in MF-319 for 15-20 sec
    (more detailed lift-off processing is presented in Appendix I.3.)
    DI rinse and N_2 blow-dry
2b. Ohmic contact metal depositon
    O_2 plasma descum (900 mT, 10 W), 2 min
    Etch in 10 % NH_4OH:H_2O for 15 sec.
    DI rinse and N_2 blow-dry
    Deposit Ti/Al/Ni/Au (20 nm/120 nm/40 nm/80 nm)
    Soak in acetone for 1 min.
    Spray with acetone
    IPA rinse and N_2 blow-dry
    Inspect, repeat acetone spray as necessary, swab in extreme cases
    Soak in PG Remover for 5 minutes
    IPA rinse
    DI rinse and N_2 blow-dry
    Anneal in N_2, 30 sec, 900 ℃(RTA)
3. Process Control Tests

Measure specific contact resistance (TLM)
Test saturation current between ohmic contacts
Test mesa to mesa isolation current
Repeat anneal if R_C is off-spec, or mesa etch if isolation is off-spec

4. Passivation
   O_2 plasma descum (900 mT, 10 W), 2 min.
   10 % NH_4OH:H_2O for 1 min.
   DI rinse and N_2 blow-dry
   PECVD SiN_x (100 nm)

5a. Lithography for gate opening
   Spin S1811, 4000 RPM, 30 sec.
   Bake at 105 ℃for 1 min. (hot plate)
   Expose for 35 sec. with recess mask
   Develop in MF-319 for approx. 25-30 sec.
   DI rinse and N_2 blow-dry
   Post bake at 105 ℃for 2 min. (hot plate)

5b. Gate opening etch
   RIE etch SiN_x in SF_6 (26 sccm/50 mT/44W), 120 nm/min.
   Acetone rinse
   IPA rinse and N_2 blow-dry

5c. Lithography for gate metal spin LOR7B, 4000 rpm, 30 sec.
   Bake at 190 ℃for 5 min. (hot plate)
   Spin S1805, 4000 rpm, 30 sec.
   Bake at 105 ℃for 1 min. (hot plate)
   Expose for 15 sec. at 15 mW/cm^2 with gate mask
   Develop in MF-319 for 15-20 sec.
   DI rinse and N_2 blow-dry

5d. Gate metal deposition
   O_2 plasma descum (900 mT, 10 W), 2 min.
   10 % NH_4OH:H_2O for 15 sec.
   DI rinse and N_2 blow-dry
   Deposit Ni/Au (20 nm/200 nm)
   Soak in acetone for 1 min.
   Spray with acetone
   IPA rinse and N_2 blow-dry
   Inspect, repeat acetone spray as necessary, swab in extreme cases
   Soak in PG Remover for 5 min.
   IPA rinse
   DI rinse and N_2 blow-dry

6a. Lithography for contact window
   Spin S1811, 4000 RPM, 30 sec.
   Bake at 105 ℃for 1 min. (hot plate)
   Expose for 35 sec. with NCD contact mask
   Develop in MF-319 for approx. 20-25 sec.
   DI rinse and N_2 blow-dry

Post bake at 105 ℃for 2 min. (hot plate)

6b. Etch contact window

RIE etch SiN_x in SF_6 (26 sccm/50 mT/44W), 120 nm/min.
Soak in acetone for 5 min.
IPA rinse and N_2 blow-dry

7a. Lithography for final metal

4000 rpm LOR7B
Bake at 190 and for 5 min. (hot plate)
4000 rpm S1805
Bake at 105 ℃for 1 min. (hot plate)
Exposure for 15 sec. with overlay mask
Develop in MF-319 for 15-20 sec.
DI rinse and N_2 blow-dry

7b. Final metal deposition

O_2 plasma descum (900 mT, 10 W), 2 min.
Ti/Pt/Au (20 nm/30 nm/300 nm)
Soak in acetone for 1 min.
Spray with acetone
IPA rinse and N_2 blow-dry
Inspect, repeat acetone spray as necessary, swab in extreme cases
Soak in PG Remover for 5 minutes
IPA rinse
DI rinse and N_2 blow-dry

8. Process Control Tests

Measure V_{DS}-I_{DS} and V_{GS}-I_{DS} (verify gate modulation, pinch-off, and I_{DS} saturation)

III.2 Process for Diamond HEMT:

0. Wafer cleaning

Acetone rinse
IPA rinse and N_2 blow-dry

1a. Lithography for mesa level (Note: Steps 1 and 2 are interchangeable)

spin S1818, 4000 RPM, 30 sec.
Bake at 105 ℃for 2 min. (hot plate)
Expose for 70 sec.
Develop in MF-319 for approx. 40-45 sec. with mesa mask
DI rinse and N_2 blow-dry
Post bake at 90 ℃for 10 min. (hot plate)

1b. Dry etch for mesa formation

ICP Etch in Cl_2/Ar (10/5 sccm, 5 mTorr, 150 W ICP, 40 W RF), approx. 60 nm/min.

1c. Wafer cleaning

Acetone soak 5 min.
Acetone spray/swab as necessary

IPA rinse and N_2 blow-dry

2a. Lithography for ohmic level

spin LOR7B, 4000 rpm, 30 sec.
Bake at 190 ℃for 5 min. (hot plate)
spin S1805, 4000 rpm, 30 sec.
Bake at 105 ℃for 1 min. (hot plate)
Expose for 15 sec. at 15 mW/cm^2 with ohmic mask
Develop in MF-319 for 15-20 sec.
DI rinse and N_2 blow-dry

2b. Ohmic contact metal depositon

O_2 plasma descum (900 mT, 10 W), 2 min.
Etch in 10 % NH_4OH:H_2O for 15 sec.
(alternative etch: 10 % HCl, 30 sec.)
DI rinse and N_2 blow-dry
Deposit Ti/Al/Ni/Au (20 nm/120 nm/40 nm/80 nm)
Soak in acetone for 1 min.
Spray with acetone
IPA rinse and N_2 blow-dry
(alternative lift-off: MF319 dip, 30 sec., DI rinse, N_2 dry)
Inspect, repeat acetone spray as necessary, swab in extreme cases
Soak in PG Remover for 5 minutes
IPA rinse
DI rinse and N_2 blow-dry
Anneal in N_2, 30 sec, 900 ℃(RTA)

3. Process Control Tests

Measure specific contact resistance (TLM)
Test saturation current between ohmic contacts
Test mesa to mesa isolation current
Repeat anneal if R_C is off-spec, or mesa etch if isolation is off-spec

4. Deposit Oxide (SiO_2)

O_2 plasma descum (500 mT, 10 W), 2 min.
10 % NH_4OH:H_2O for 1 min.
DI rinse and N_2 blow-dry
PECVD SiO_2 (50 nm)

5a. Lithography for ohmic contact window

spin S1811, 4000 RPM, 30 sec.
Bake at 105 ℃for 1 min. (hot plate)
Expose for 35 sec. with NCD contact mask
Develop in MF-319 for approx. 20-25 sec.
DI rinse and N_2 blow-dry
Post bake at 105 ℃for 2 min. (hot plate)

5b. Window opening etch

RIE etch SiN_x in SF_6 (26 sccm/50 mT/44 W), 120 nm/min.
Acetone rinse
IPA rinse and N_2 blow-dry

6. Deposit NCD
7. Deposit Nitride 2
    O_2 plasma descum (500 mT, 10 W), 2 min.
    10 % NH_4OH:H_2O for 1 min.
    DI rinse and N_2 blow-dry
    PECVD SiN_x (100 nm)

8a. Lithography for gate and contact window opening
    Spin S1811, 4000 RPM, 30 sec.
    Bake at 105 ℃for 1 min. (hot plate)
    Expose for 35 sec. with NCD contact mask
    Expose for 35 sec. with recess mask
    Develop in MF-319 for approx. 20-25 sec.
    DI rinse and N_2 blow-dry
    Post bake at 105 ℃for 2 min. (hot plate)

8b. Etch gate recess and contact window opening
    Etch Nitride 2 in SF_6 (26 sccm/50 mT/44 W), 120 nm/min.
    Etch NCD in O_2 (100 sccm/50 mT/200 W), approx. 10 nm/min.
    Etch Nitride 1 in SF_6 (26 sccm/50 mT/44 W), 120 nm/min.

9a. Lithography for gate metal
    Spin LOR7B, 4000 rpm, 30 sec.
    Bake at 190 ℃for 5 min. (hot plate)
    Spin S1805, 4000 rpm, 30 sec.
    Bake at 105 ℃for 1 min. (hot plate)
    Expose for 15 sec. at 15 mW/cm^2 with gate mask
    Develop in MF-319 for 15-20 sec.
    DI rinse and N_2 blow-dry

9b. Gate metal deposition
    O_2 plasma descum (900 mT, 10 W), 2 min.
    10 % NH_4OH:H_2O for 15 sec.
    DI rinse and N_2 blow-dry
    Deposit Ni/Au (20 nm/200 nm)
    Soak in acetone for 1 min.
    Spray with acetone
    IPA rinse and N_2 blow-dry
    Inspect, repeat acetone spray as necessary, swab in extreme cases
    Soak in PG Remover for 5 minutes
    IPA rinse
    DI rinse and N_2 blow-dry

11a. Lithography for final metal
    4000 rpm LOR7B
    Bake at 190 ℃for 5 min. (hot plate)
    4000 rpm S1805
    Bake at 105 ℃for 1 min. (hot plate)
    Exposure for 15 sec. with overlay mask
    Develop in MF-319 for 15-20 sec.

DI rinse and N_2 blow-dry

11b. Final metal deposition

O_2 plasma descum (900 mT, 10 W), 2 min.
Ti/Pt/Au (20 nm/30 nm/300 nm)
Soak in acetone for 1 min.
Spray with acetone
IPA rinse and N_2 blow-dry
Inspect, repeat acetone spray as necessary, swab in extreme cases
Soak in PG Remover for 5 minutes
IPA rinse
DI rinse and N_2 blow-dry

12. Process Control Tests

Measure V_{DS}-I_{DS} and V_{GS}-I_{DS} (verify gate modulation, pinch-off, and I_{DS} saturation)

Appendix IV
Characterization Programs
IV.1 C-V analysis with HP 4275

```
1  bool doCV (int frequency, double CV_Vstart, double CV_Vstop) {
2
3      ofstream outfile;
4      int status, j=0;
5      int K230Range, temp, temp1, LCRrange;
6      double freq;
7      String temp_string="", temp_freq="";
8      char value[80]="";
9
10     //determine frequency of CV measurement
11     switch (frequency) {
12         case 0: freq = 2*M_PI*1e4 ; temp = 11; break;
13         case 1: freq = 2*M_PI*3e4 ; temp = 12; break;
14         case 2: freq = 2*M_PI*5e4 ; temp = 13; break;
15         case 3: freq = 2*M_PI*1e5 ; temp = 14; break;
16         case 4: freq = 2*M_PI*3e5 ; temp = 15; break;
17         case 5: freq = 2*M_PI*5e5 ; temp = 16; break;
18         case 6: freq = 2*M_PI*1e6 ; temp = 17; break;
19         case 7: freq = 2*M_PI*3e6 ; temp = 18; break;
20         case 8: freq = 2*M_PI*5e6 ; temp = 19; break;
21         case 9: freq = 2*M_PI*1e7 ; temp = 20; break;
22         default: break;
23     }
24
25     if ( (Form1->fmCV_useK230->Checked) && ( ! abortMeasure ) )
           {
26         //find range of voltage measurement for keithley 230
27         if ( abs(CV_Vstart) > abs(CV_Vstop) )
28             temp1 = abs(CV_Vstart);
29         else
30             temp1 = abs(CV_Vstop);
31         if (temp1 >= 10) K230Range = 4;
32         else if ((temp1 >= 1) && (temp1 < 10)) K230Range = 3;
33         else if ((temp1 >= 0.1) && (temp1 < 1)) K230Range = 2;
34         else if (temp1 < 0.1) K230Range = 1;
35
36         sendMachine(K230_id, "R" + IntToStr(K230Range));
37         sendMachine(K230_id, "I" +
38             IntToStr(Form1->fmCV_Ilimit->ItemIndex));
39         sendMachine(K230_id, "P0T2V0F1X");
```

```
40          //see Keithley 230 manual for program codes
41      } else if ( ! abortMeasure ) {
42          //set keithley 237
43          sendMachine(K237_id, "F0,0X");
44          ibrd(K237_id, value, 23);
45          sendMachine(K237_id, "L1e-6,4X");
46          ibrd(K237_id, value, 23);
47          sendMachine(K237_id, "B0,4,0X");
48          ibrd(K237_id, value, 23);
49          sendMachine(K237_id, "R1X");
50          ibrd(K237_id, value, 23);
51          sendMachine(K237_id, "N1X");
52          ibrd(K237_id, value, 23);
53      } // end if
54
55      //determine Capacitance Range
56      sendMachine(HP4275_id, "F"+IntToStr(temp));//manual range
57      sendMachine(HP4275_id, "R"+IntToStr(LCRrange));
58      // LCRrange is integer between 11 and 20
59      if (Form1->fmCV_HiRes->Checked)
60          sendMachine(HP4275_id, "H1");
61      else
62          sendMachine(HP4275_id, "H0");
63
64      sendMachine(HP4275_id, "A2B3C3T3");
65
66      if ( CV_Vstart == CV_Vstop ) {
67          //No measurement performed
68      } else {
69          for (double i=CV_Vstart;
70              (CV_Vstart > CV_Vstop) ?
71                  i>=CV_Vstop :
72                  i<=CV_Vstop;
73              (CV_Vstart>CV_Vstop) ?
74                  i-=CV_Vstep :
75                  i+=CV_Vstep)
76          {
77              if (abortMeasure) {
78                  AbortMeasurement();
79                  outfile.close();
80                  return false;
81              }
82
83              if(Form1->fmCV_useK230->Checked) {
84                  sendMachine(K230_id, "V" + FloatToStr(i) + "X");
85              } else {
86                  sendMachine(K237_id, "B"+FloatToStr(i)+",4,0X");
```

```
87                  ibrd(K237_id, value, 23);
88              }
89
90              Sleep(CV_TimeDelay);
91              sendMachine(HP4275_id, "E");
92              Sleep(CV_TimeDelay);
93              ibrd(HP4275_id, value,34);
94              temp_string = value;
95
96              CV_Voltage[j] = i;
97              CV_Data[j]=atof(temp_string.SubString(6,12).c_str())
                    ;
98              CV_OneOverCSqData[j] = 1 / (CV_Data[j]*CV_Data[j]);
99              CV_Conductance[j] =
100                 atof(temp_string.SubString(21,12).c_str());
101             CV_Theta[j]=(-1)*atan((freq*CV_Data[j])/
102                                   CV_Conductance[j])*(180/M_PI)
                                      ;
103
104             j++;
105         } //end for
106
107         CalcNd(CV_Vstart, CV_Vstop);
108
109     } // end if
110
111     sendMachine(HP4275_id,"T1");
112     if(Form1->fmCV_useK230->Checked)
113         sendMachine(K230_id, "V0F0X");
114     else {
115         sendMachine(K237_id, "B0,4,0XN0X");
116         ibrd(K237_id, value, 23);
117     }
118     Sleep(1000);
119     return true;
120 } // end function
121
122 // Carrier concentration analysis, as given in Schroder
123 void CalcNd(double CV_Vstart, double CV_Vstop) {
124     double ContactAreaValue;
125     double Eo = 8.85E-14;
126     double Q = 1.602E-19;
127     double V[MAX_NUM_PTS];
128     double correction_factor;
129
130     if (ContactDimension == AREA)
131         ContactAreaValue = ContactSize * 0.00000001;
```

```
132     else {
133         ContactAreaValue = M_PI * pow( (ContactSize / 2),2)*1e
                -8;
134     }
135
136     for (int i = 0; i < CV_NumPts; i++) {
137         if ( CV_Vstart > CV_Vstop )
138             V[i] = CV_Vstart - i * CV_Vstep;
139         else
140             V[i] = CV_Vstop - i * CV_Vstep;
141
142         CV_DepWidth[i] = 0;
143         CV_DepWidth_Corr[i] = 0;
144         CV_CarrierConcData[i] = 0;
145         CV_CarrierConcData_Method2[i] = 0;
146         CV_CarrierConcData_Method2_Corr[i] = 0;
147     }
148
149     // calculating the depletion width, in microns
150     for (int i=0; i<CV_NumPts; i++) {
151         CV_DepWidth[i] = Ks * ContactAreaValue * Eo * 10000
152                                                     / CV_Data[i
                                                        ];
153         CV_DepWidth_Corr[i] =   CV_DepWidth[i] *
154                                 pow(sin(CV_Theta[i]), 2);
155     }
156
157     // calculating carrier concentration
158     for (int i=0; i<CV_NumPts-2; i++) {
159         double deltaC = CV_Data[i]-CV_Data[i+2];
160         double delta1C2 =
161             CV_OneOverCSqData[i]-CV_OneOverCSqData[i+2];
162         double deltaV = V[i]-V[i+2];
163         double deltaTheta = CV_Theta[i]-CV_Theta[i+2];
164         double Factor =Q*Ks*Eo*ContactAreaValue*ContactAreaValue
                ;
165
166         if (delta1C2 < 0) delta1C2 = -delta1C2;
167
168         if  (deltaC != 0) {
169             CV_CarrierConcData[i] =
170             (2 * deltaV) / (Factor * delta1C2);
171
172             CV_CarrierConcData_Method2[i] =
173             -(pow(CV_Data[i+1], 3) * deltaV) / (Factor * deltaC)
                    ;
174
```

```
175                 correction_factor =
176                     pow(sin(CV_Theta[i+1]),4) *
177                     (deltaC - ( 2*CV_Data[i+1]*deltaTheta*
178                         cos(CV_Theta[i+1]) / sin(CV_Theta[i+1]))) ;
179
180                 CV_CarrierConcData_Method2_Corr[i] =
181                 -(pow(CV_Data[i+1], 3) / Factor) / correction_factor
                        ;
182             } else
183                 CV_CarrierConcData[i] =
184                 CV_CarrierConcData_Method2[i] =
185                 CV_CarrierConcData_Method2_Corr[i] = 1000000000000;
186         }
187 }
```

IV.2 Pulsed forward blocking mode breakdown voltage measurement

```
1  int Breakdown() {
2      int status;
3      char value[80]="";
4
5      //set keithley 237
6      SendMachine(K237id, "F0,1X");
7      ibrd(K237id, value, 23);
8      SendMachine(K237id, "B0,0,0X");
9      ibrd(K237id, value, 23);
10     SendMachine(K237id, "L" + FloatToStr(Compliance) + ",0X");
11     ibrd(K237id, value, 23);
12     SendMachine(K237id, "O1X");
13     ibrd(K237id, value, 23);
14     if(Form1->btnStair->Checked) {
15         SendMachine(K237id, "Q1," + FloatToStr(Vstart) + ","
16         + FloatToStr(Vend) + "," +
17         FloatToStr(Vstep) + "," + "0,100X");
18     } else if(Form1->btnPulsed->Checked) {
19         SendMachine(K237id, "Q4," + FloatToStr(Vstart) + ","
20         + FloatToStr(Vend) + "," +
21         FloatToStr(Vstep) + "," + "4," + FloatToStr(Ton) +
22         "," + FloatToStr(Toff) + "X");
23     }
24
25     ibrd(K237id, value, 23);
26     SendMachine(K237id, "R1X");
27     ibrd(K237id, value, 23);
28     SendMachine(K237id, "N1X");
29     ibrd(K237id, value, 23);
30     SendMachine(K237id, "T4,0,0,0X");
31     ibrd(K237id, value, 23);
32     SendMachine(K237id, "H0X");
33
34     return status;
35 }
```

IV.3 Thermally stimulated current measurement

```
1  //Thread 1 - Temperature control
2  DWORD CALLBACK Temperature(void* p) {
3      HDC DC = GetDC(Form1->Handle);
4
5      while(! abortMeasure) {
6          temp_read = Read_Temperature();
7          Sleep(250);
8          if (heaterOn) {
9              sendMachine(DRC91C_id, "R5" );
10             heaterOn = false;
11         }
12         if (heaterOff) {
13             sendMachine(DRC91C_id, "R0" );
14             heaterOff = false;
15         }
16     }
17     ReleaseDC(Form1->Handle, DC);    // release thread
18
19     return 0;
20 }  // end function
21
22 //Thread 2 - Data recording
23 DWORD CALLBACK Measure(void* p) {
24     HDC DC = GetDC(Form1->Handle);
25
26     ofstream outfile;
27     String temp_string="";
28     char value[80]="";
29     double current1, current2;
30
31     outfile.open("D1-noisemon.txt", ios_base::app );
32     outfile << "Date" << "\t" << "Time" << "\t"
33             << "Temp_(K)" <<  "\t" << "I_K6517_(A)" << "\t"
34             << "V_K6517_(V)" << endl;
35     K6517_On();
36
37     while(! abortMeasure) {
38         sendMachine(K6517_id, "X");
39         ibrd(K6517_id, value, 16);
40         temp_string = value;
41         current1=atof(temp_string.SubString(5,12).c_str());
42         outfile << DateToStr(Date()).c_str() << "\t"
43                 << TimeToStr(Time()).c_str() << "\t"
44                 << temp_read << "\t" << current1
45                 << "\t" << K6517Bias << endl;
```

```
46                  Sleep(250);
47      }
48
49      Bias_K6517_Off();
50      outfile.close();
51      ReleaseDC(Form1->Handle, DC);    // release thread
52      return 0;
53  }  // end function
54
55  //Thread 3 - Pressure control
56  DWORD CALLBACK Pressure(void* p) {
57      HDC DC = GetDC(Form1->Handle);
58      double pressure,temp_apply=0.0;
59
60      for(double i=0; i<6; i++) {
61          //sleep for a while to make sure temp_read gets set
62          Sleep(10000);
63
64          temp_apply+=30.0;
65          if (temp_read > temp_apply) {
66
67              // bias in strong accumulation when T reaches 273
68              while(temp_read > temp_apply) {
69                  pressure = Read_Pressure();
70                  if (pressure > 0.0) {
71                      if (pressure > 6.0) {
72                          //pressure too high
73                          Bias_K237_On();
74                          Sleep(5000);
75                          Bias_K237_Off();
76                          Sleep(2000);
77                      }
78                      if (pressure < 5.0) {
79                          Bias_K230_On(20);
80                          Sleep(5000);
81                          Bias_K230_Off();
82                          Sleep(2000);
83                      }
84                  } else {
85                      // there's some error
86                  }
87              } // end while
88
89              // apply bias once desired temperature is reached
90              K6517Bias = -10;
91              Bias_K6517_On(K6517Bias);
92
```

```
93              // continue cooling down until 17 K
94              while(temp_read > 19.0) {
95                  pressure = Read_Pressure();
96                  if (pressure > 0.0) {
97                      if (pressure > 6.0) {
98                          //pressure too high
99                          Bias_K237_On();
100                         Sleep(5000);
101                         Bias_K237_Off();
102                         Sleep(2000);
103                     }
104                     if (pressure < 5.0) {
105                         Bias_K230_On(20);
106                         Sleep(5000);
107                         Bias_K230_Off();
108                         Sleep(2000);
109                     }
110                 } else {
111                     // there's some error
112                 }
113             } // end while
114
115             // wait for temperature to stabilize a bit
116             Sleep(10000);
117
118             // relieve pressure so cooling does not continue
119             Bias_K237_On();
120             Sleep(20000);
121
122             // bias device in depletion/inversion
123             K6517Bias = 10;
124             Bias_K6517_On(K6517Bias);
125             Sleep(500);
126
127             // tell Temperature to set heater power on
128             heaterOn = true;
129
130             // warm up
131             while (temp_read < 252.0);
132
133             // remove device bias
134             K6517Bias = 0;
135             Bias_K6517_On(K6517Bias);
136             Sleep(500);
137
138             // stop venting and wasting He
139             Bias_K237_Off();
```

```
140             Sleep(500);
141
142             // tell Temperature to turn heater off
143             heaterOff = true;
144             Sleep(500);
145
146         } // end if
147     } // end for
148
149     // leave He tank venting, just in case
150     Bias_K237_On();
151
152     // tell Temperature and Measure to quit
153     abortMeasure = true;
154
155     ReleaseDC(Form1->Handle, DC);    // release thread
156     return 0;
157 } // end function
```

IV.4 Exporting data from Borland C++ to Microsoft Excel

```
#include "Excel.h" //contact author for this file

void __fastcall TForm1::fmExportExcelClick(TObject *Sender) {
    if(ExcelStarted) {
        MyExcel->CloseExcel();
        delete MyExcel;
        ExcelStarted = false;
    }

    if ( FileExists( "c:\\test.xls") ) {
        OpenExcel();

        if(ExcelStarted) {
            MyExcel->Filename = AnsiString("c:\\test.xls");
            MyExcel->OpenWorkBook();

            if(MyExcel->WorkBookOpen) {
                MyExcel->VisibleSheetNo = 1;
                // Activate sheet number X
                MyExcel->ExcelVisibility = true;
                // Make excel visible to the user
            }
        }
        //insert title cells
        MyExcel->ExlCell[1][1] = Variant("Voltage [V]");
        //insert data from array
        for (int i=0; i<NumPts; i++)
            MyExcel->ExlCell[i+2][1]=Variant(Voltage[i]);
        } else {
            //Please create an empty Excel sheet
        }
}
```

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BIOGRAPHICAL SKETCH

Marko J. Tadjer was born in Sofia, Bulgaria on June 10, 1980, at 5:30 pm. As a child, he occupied himself with building cities out of his toys. In 1998, he graduated from the Technical High School of Electronics "John Atanasoff" in Sofia and accepted the Chancellor's Scholarship to attend the University of Arkansas, Fayetteville. In 2002, he graduated Magna Cum Laude with Bachelor degrees in Electrical and Computer Engineering, and a minor in Math. He received the Master's Degree in Electrical Engineering from Duke University in 2004. Since 2005, he has been researching wide bandgap semiconductor devices at the Power Electronics Branch of the United States Naval Research Laboratory in Washington, DC. Simultaneously, he has been enrolled at the Department of Electrical and Computer Engineering at the University of Maryland, College Park, where he expects to receive the Doctor of Philosophy degree in 2010. His research activities continue with a post-doctoral position in the High Speed Electronics Laboratory at the Polytechnic University of Madrid.